

Prior Art

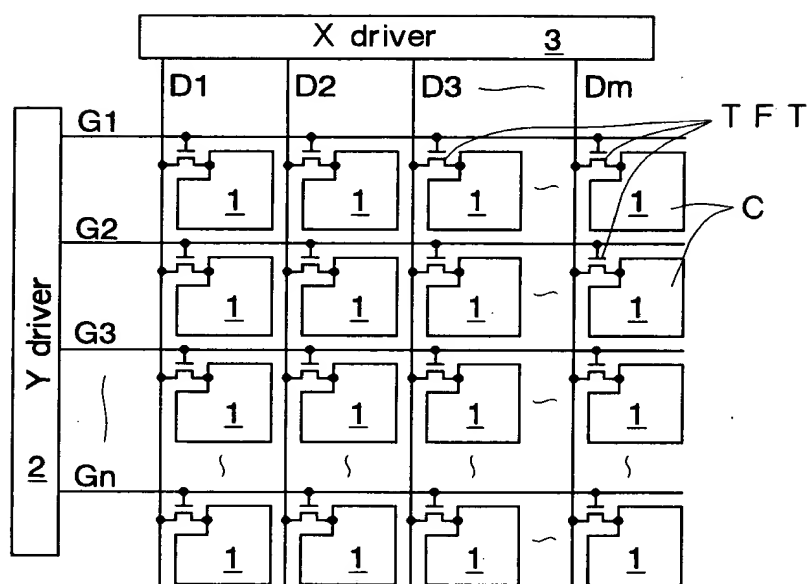


Fig. 1

Prior Art

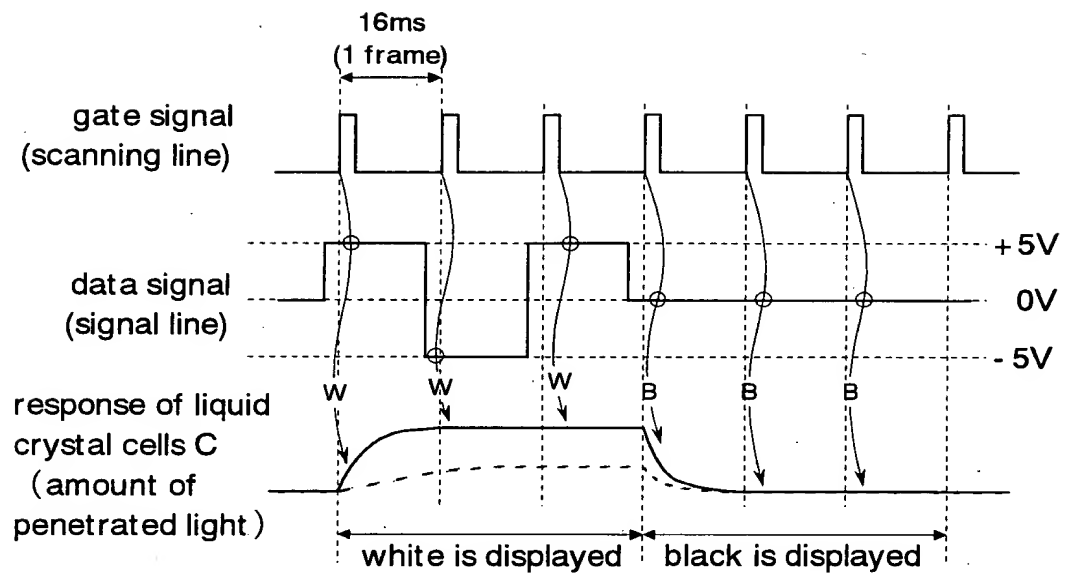


Fig. 2

Prior Art

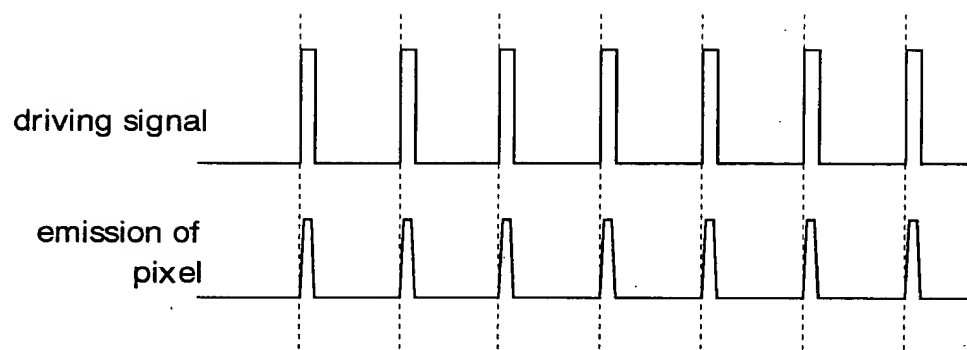


Fig. 3

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Prior Art

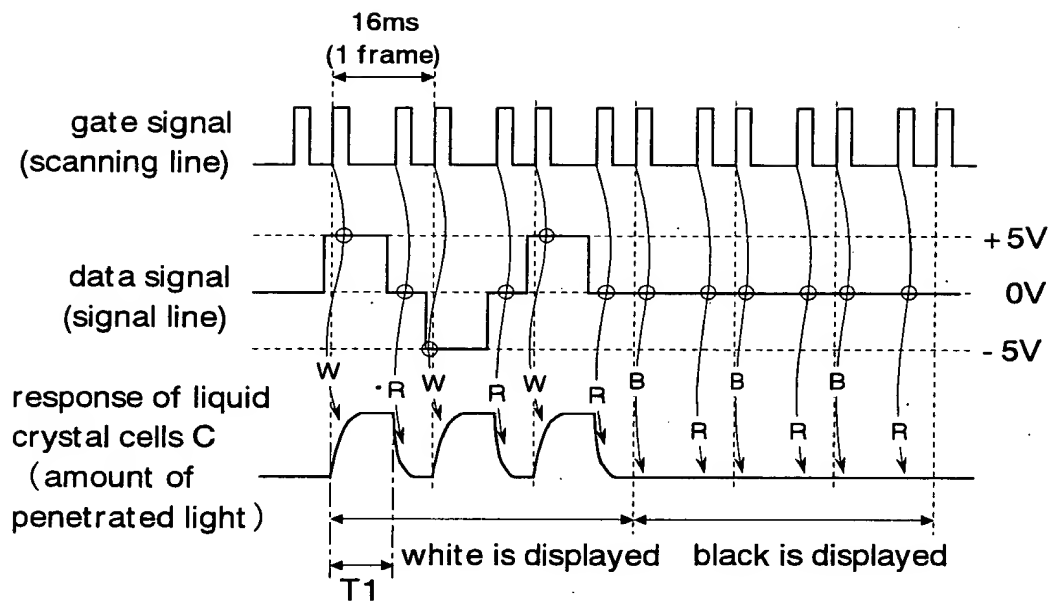


Fig. 4

Prior Art

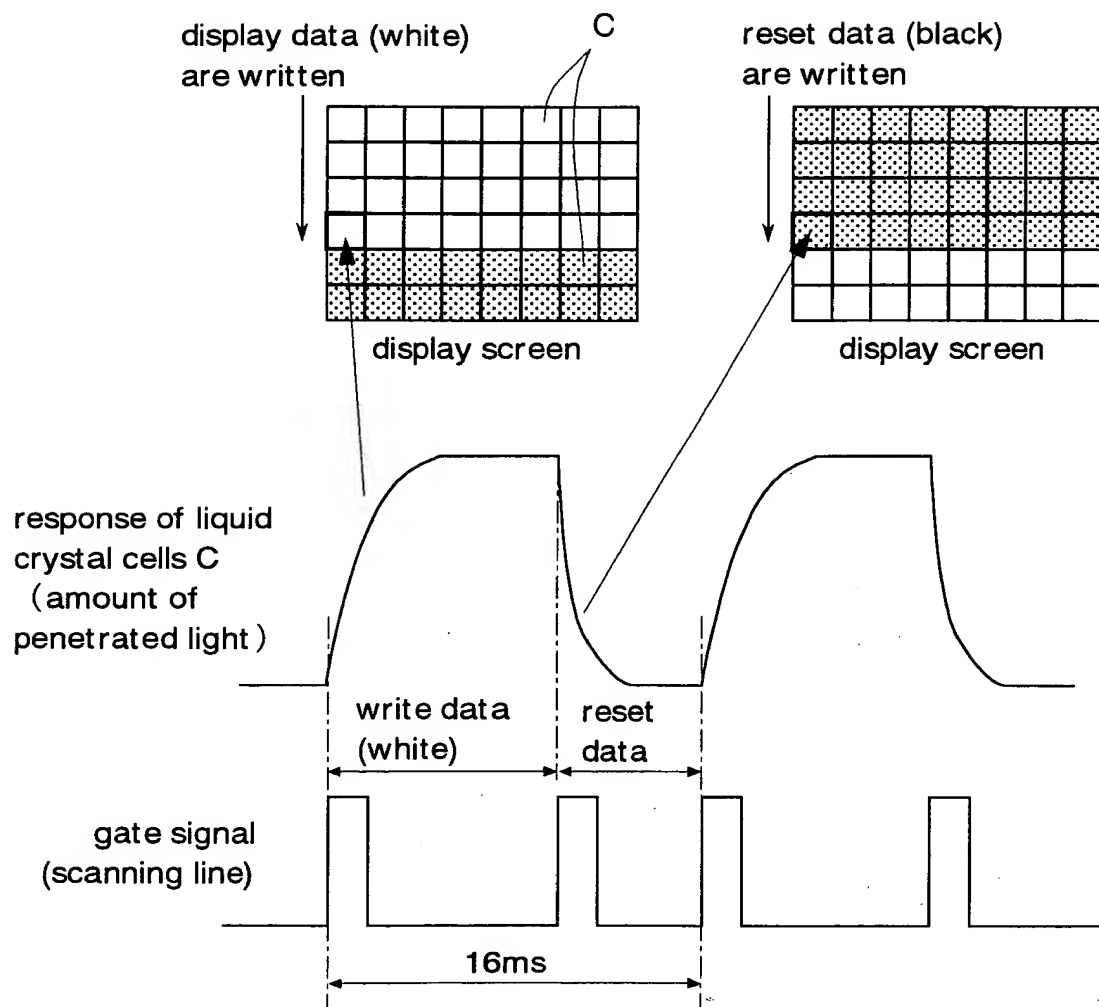


Fig. 5

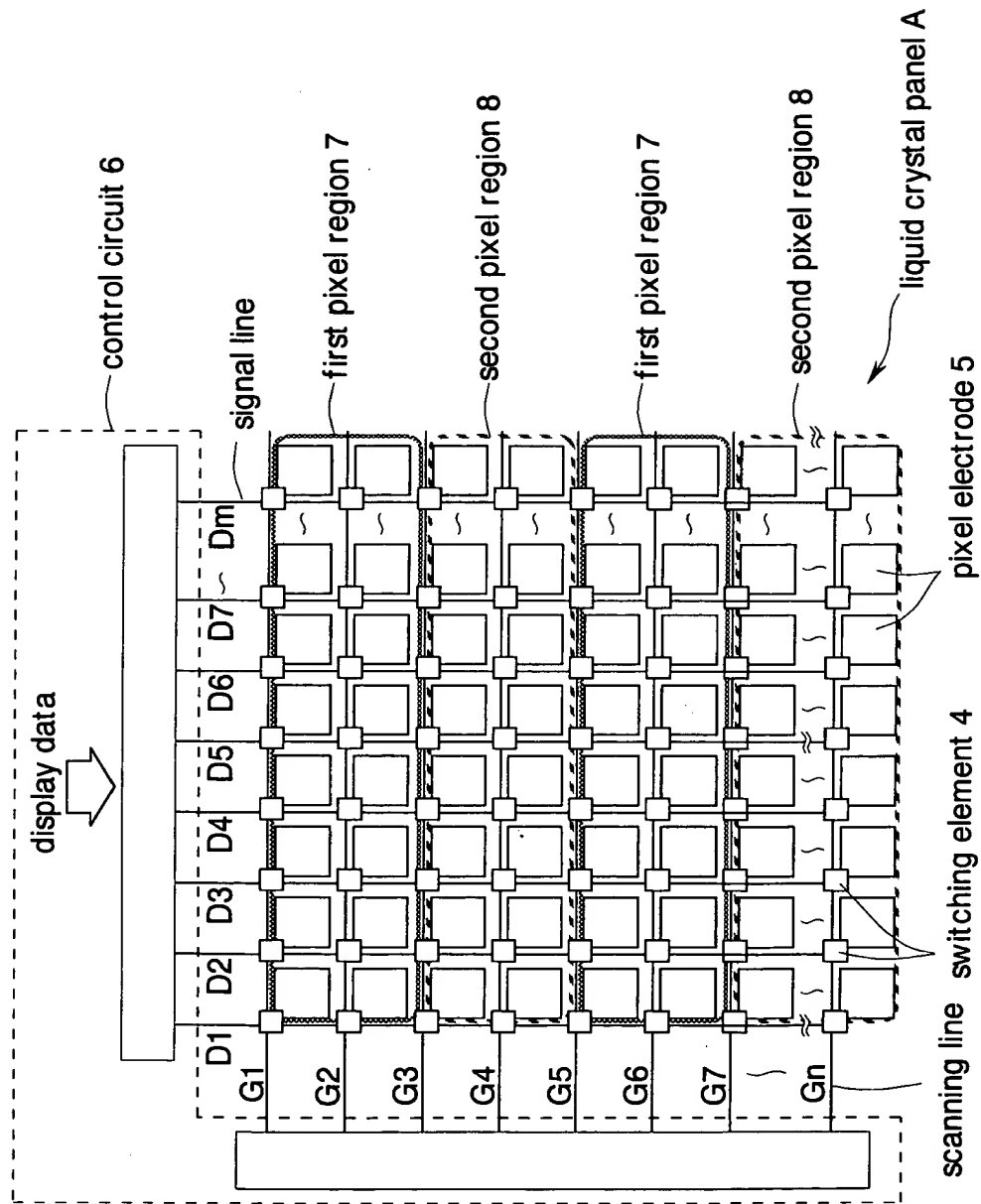


Fig. 6

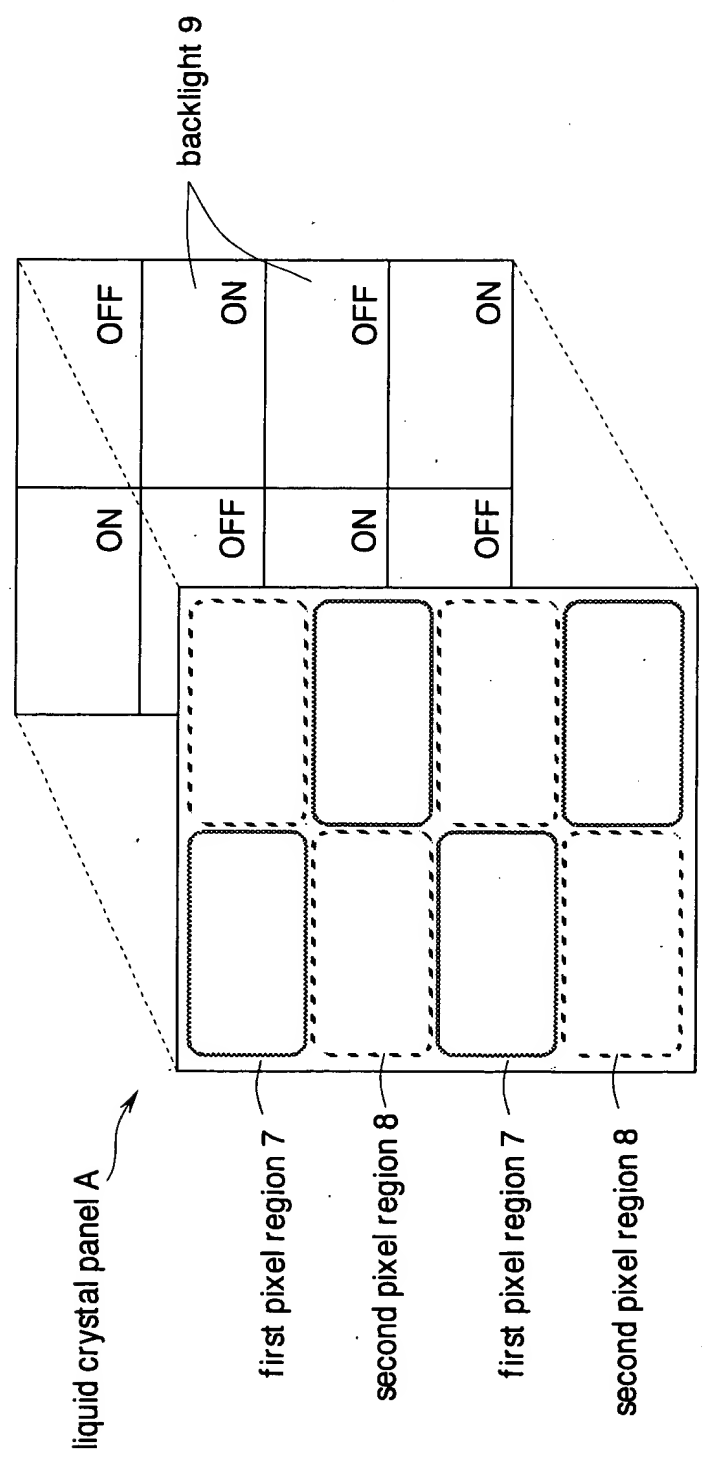


Fig. 8

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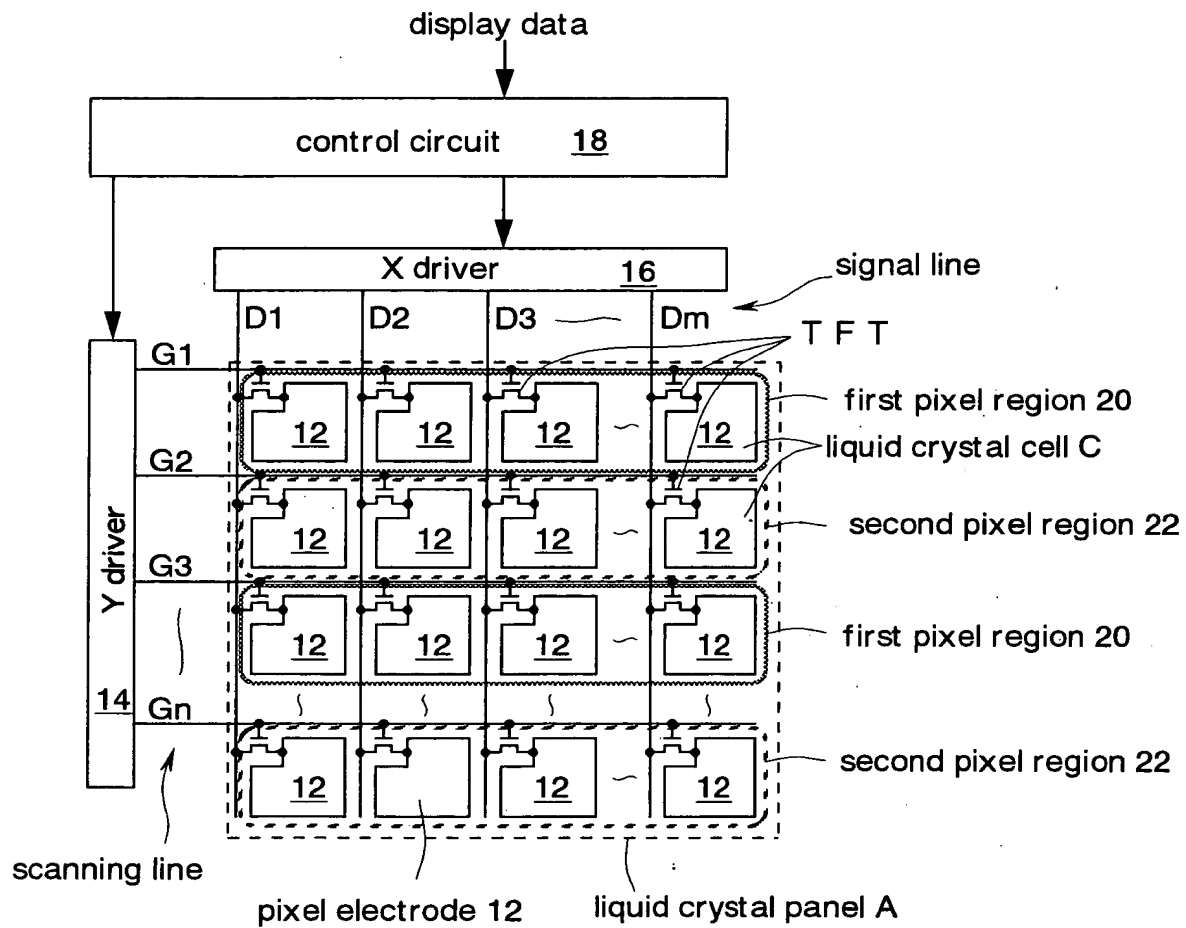
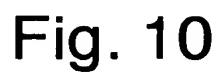


Fig. 9



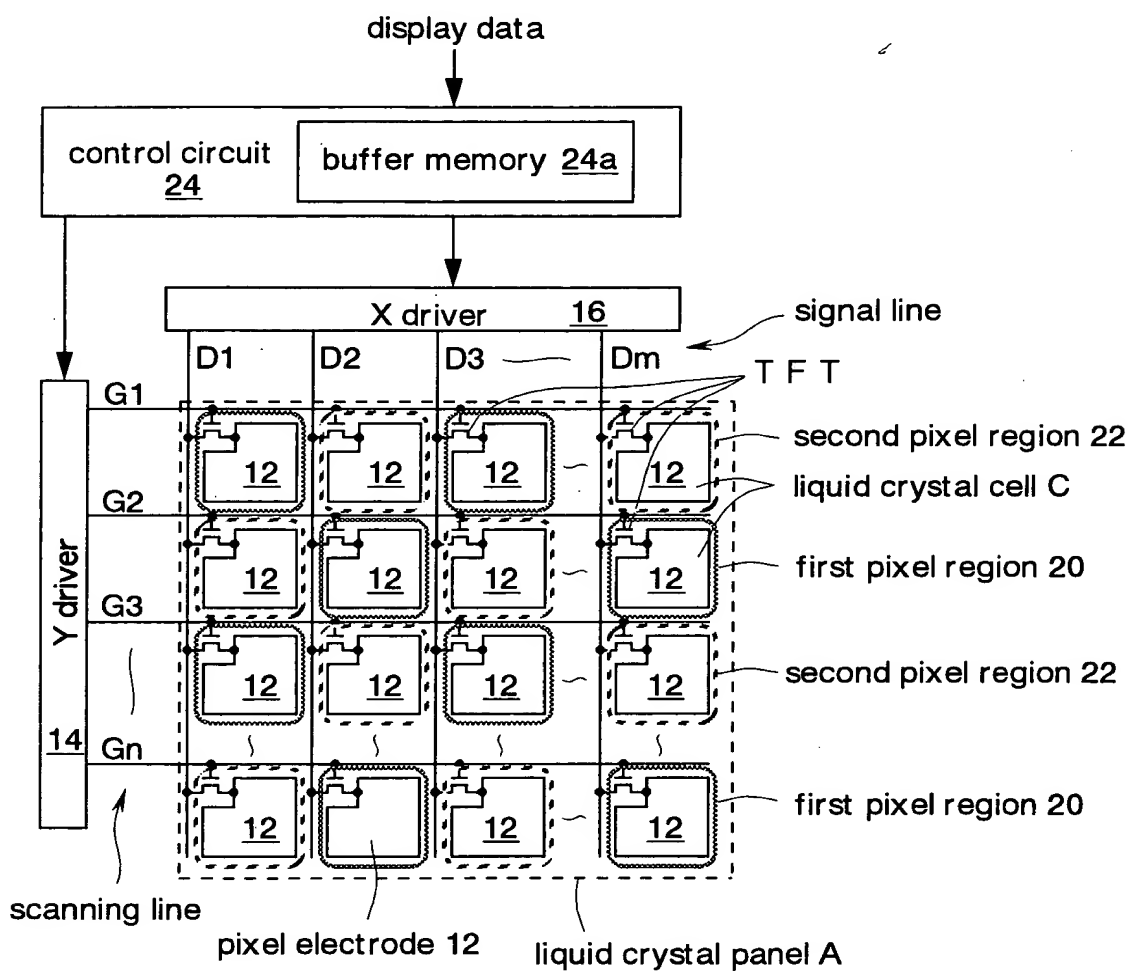


Fig. 11

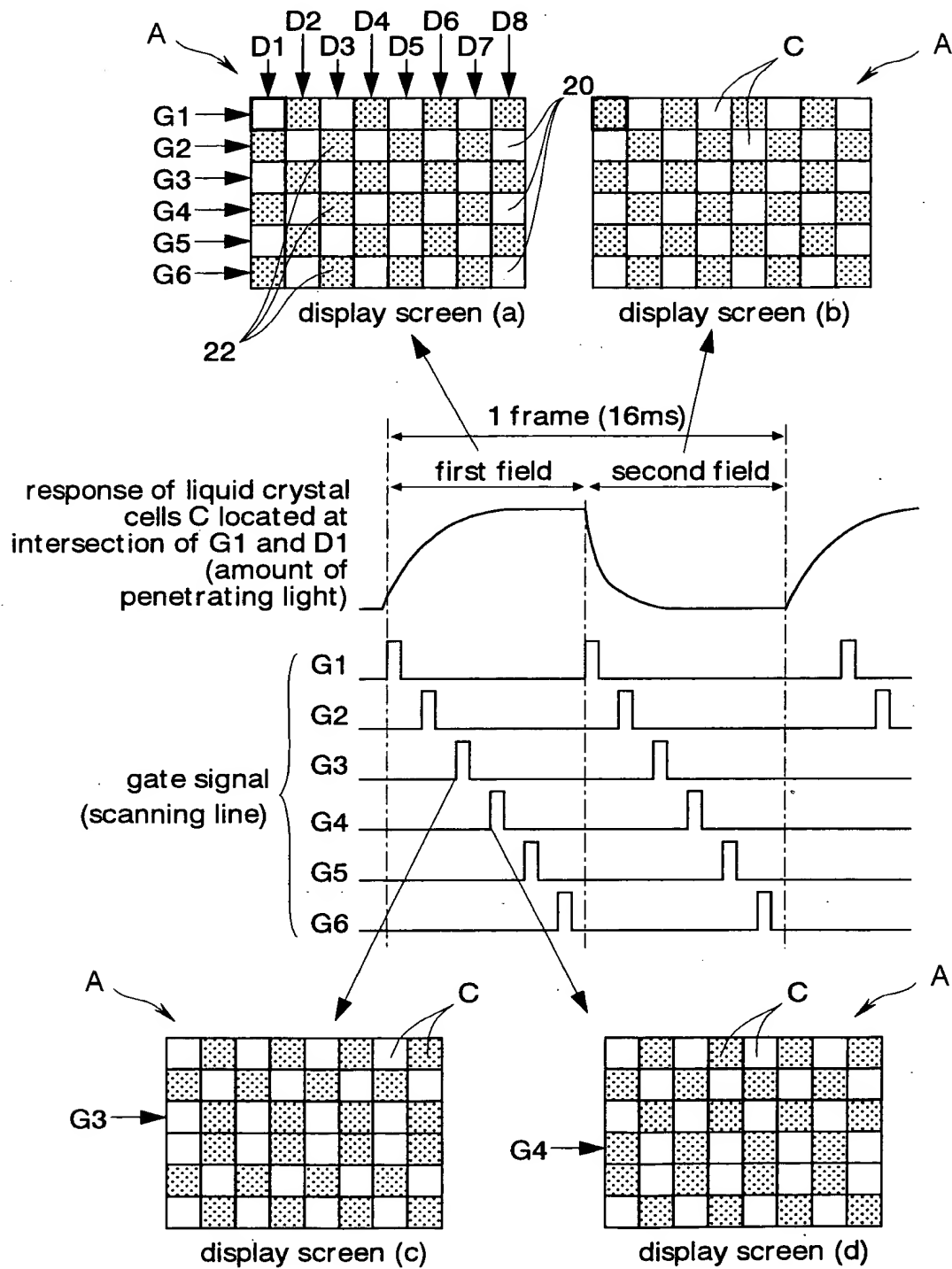


Fig. 12

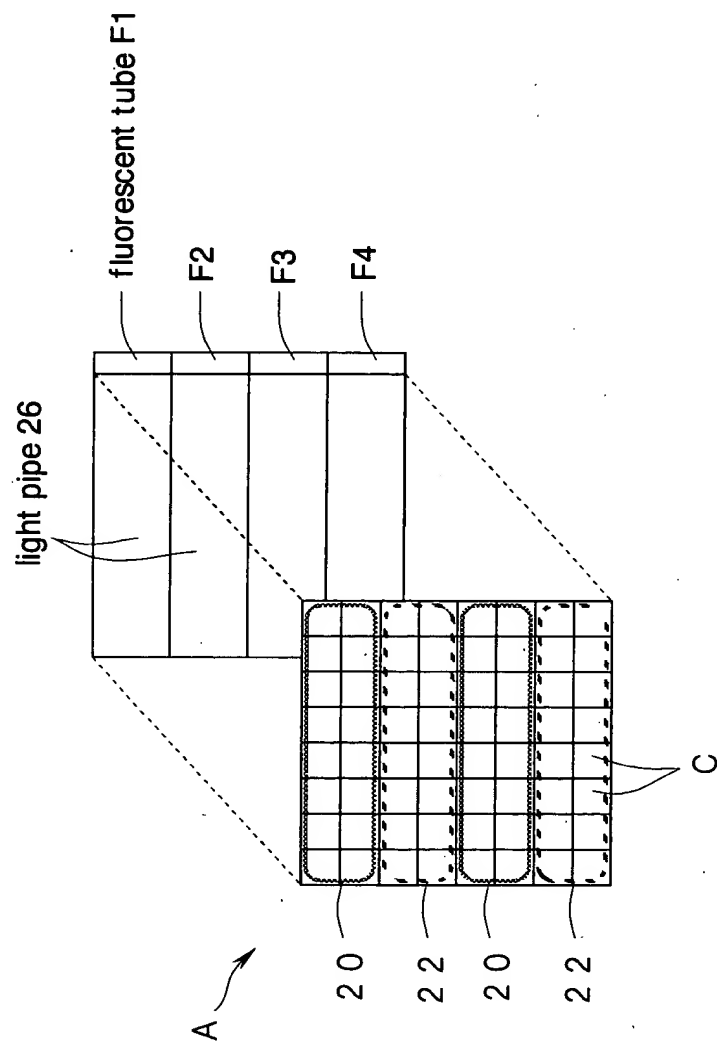


Fig. 13

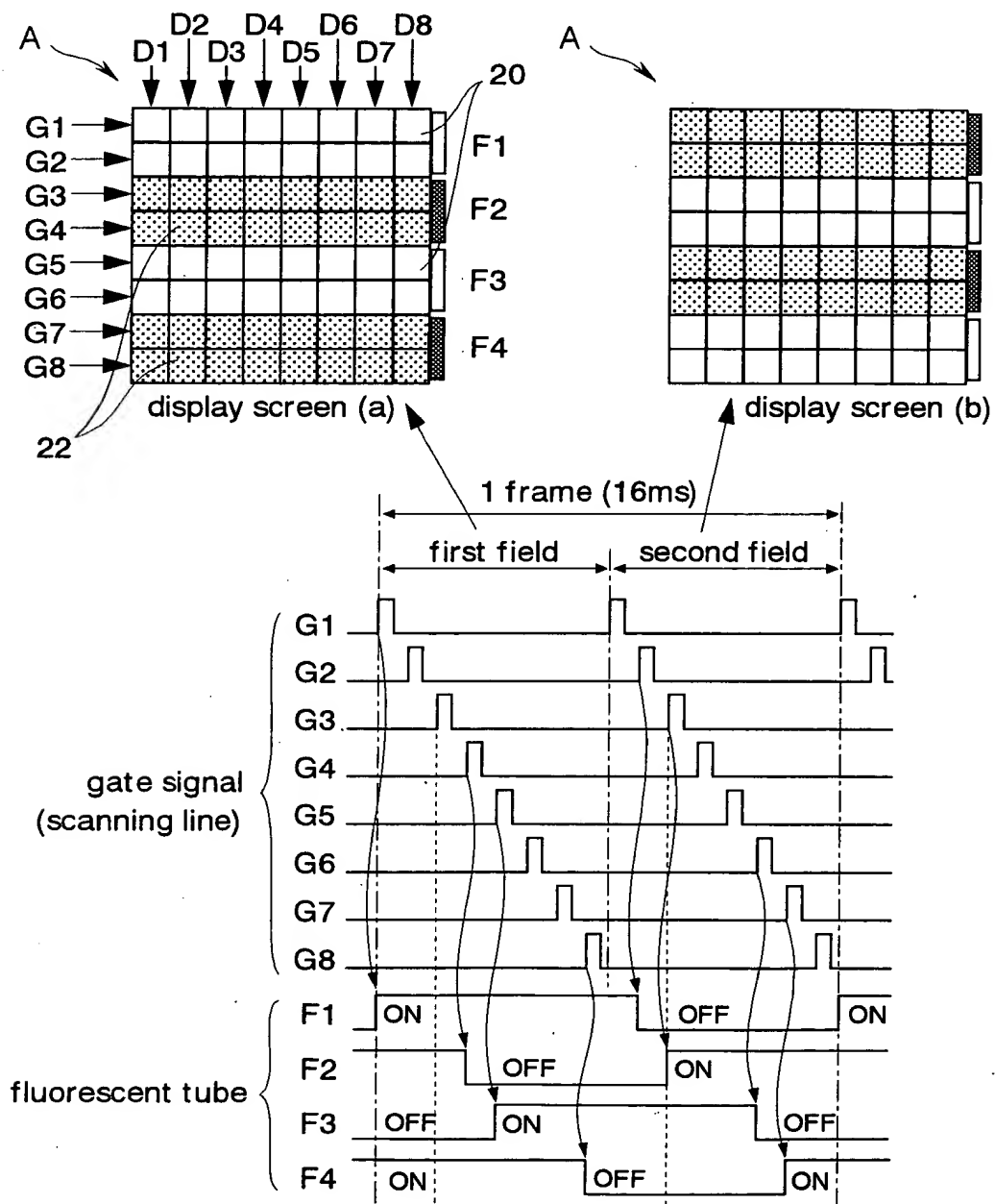
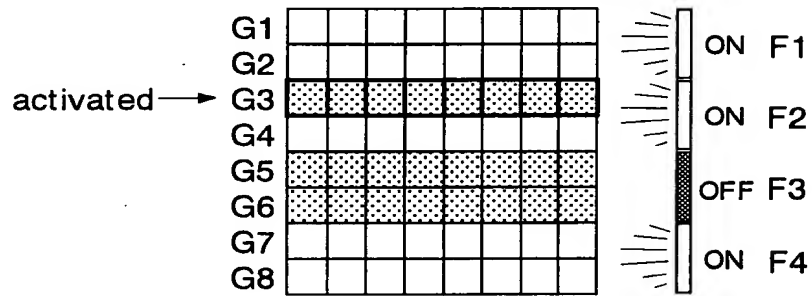
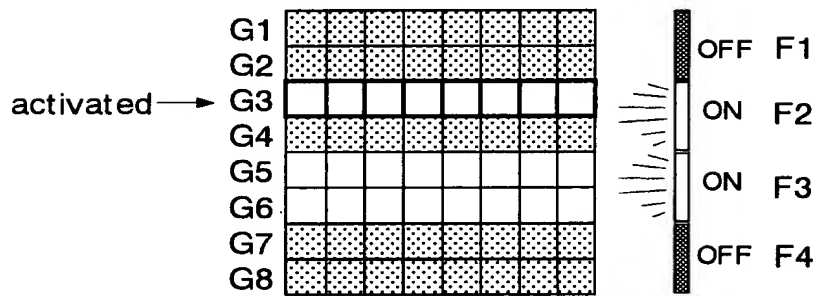


Fig. 14

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(a)



(b)

Fig. 15

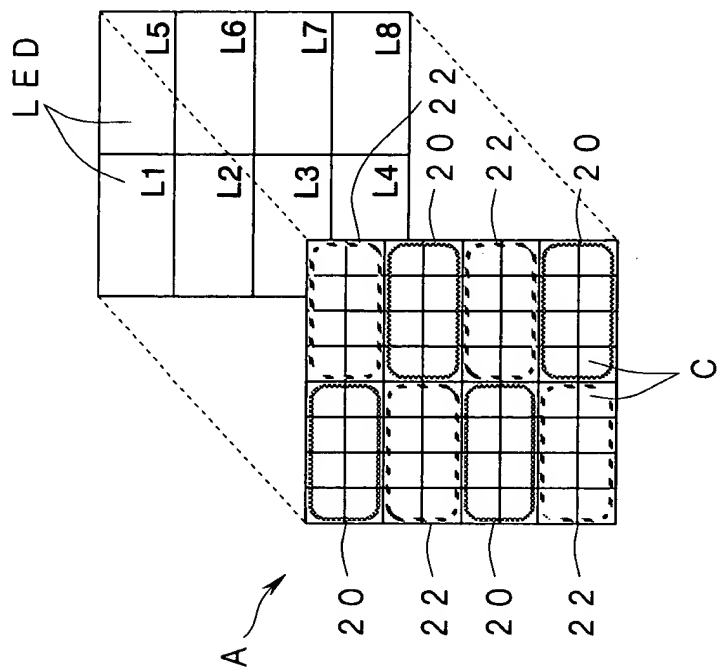


Fig. 16

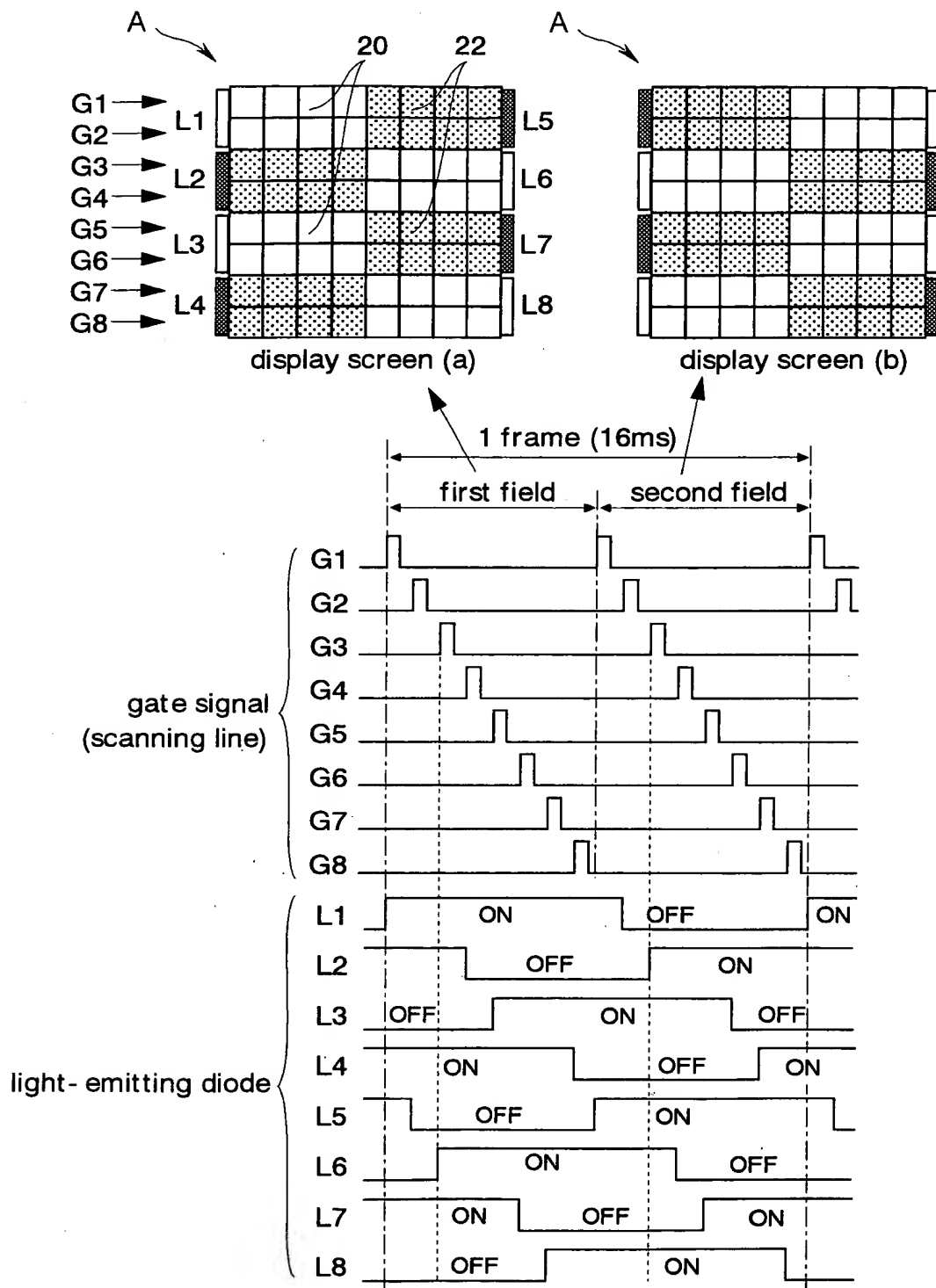


Fig. 17

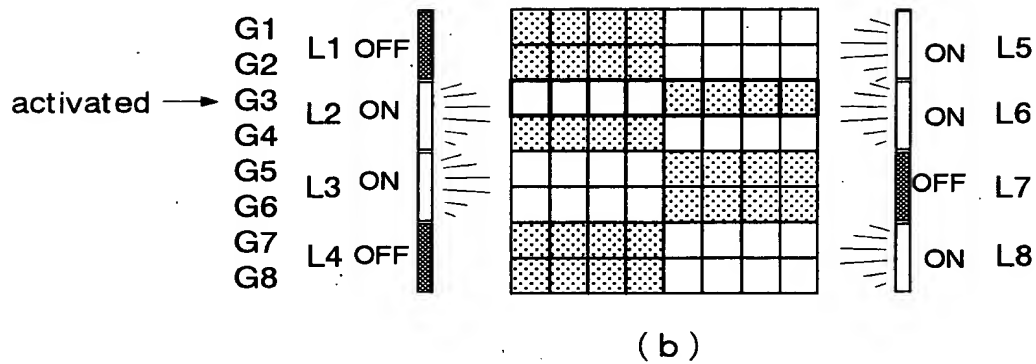
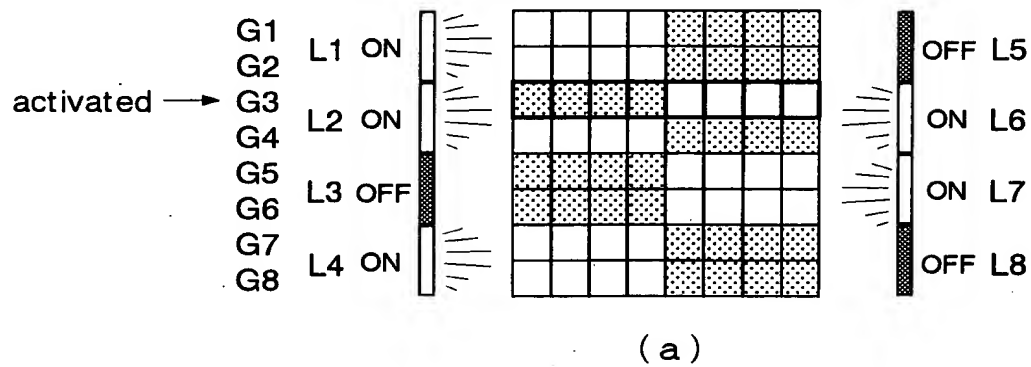


Fig. 18

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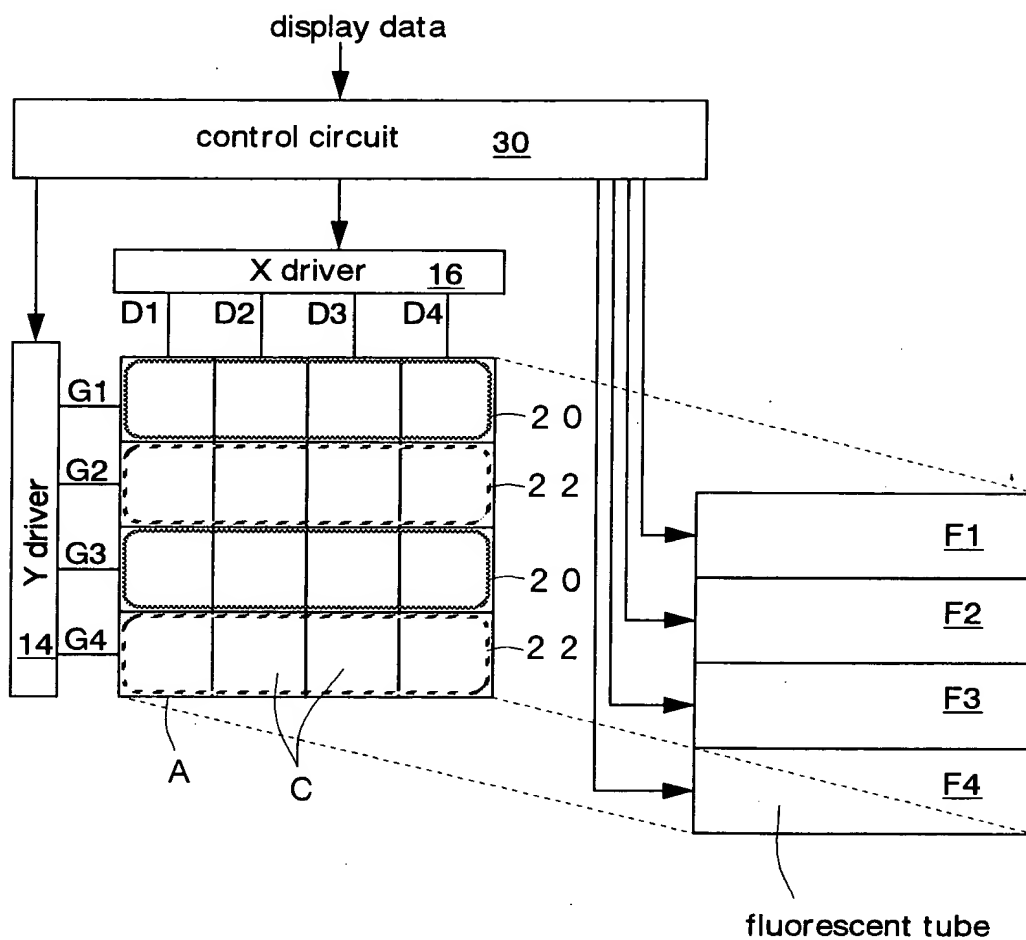


Fig. 19

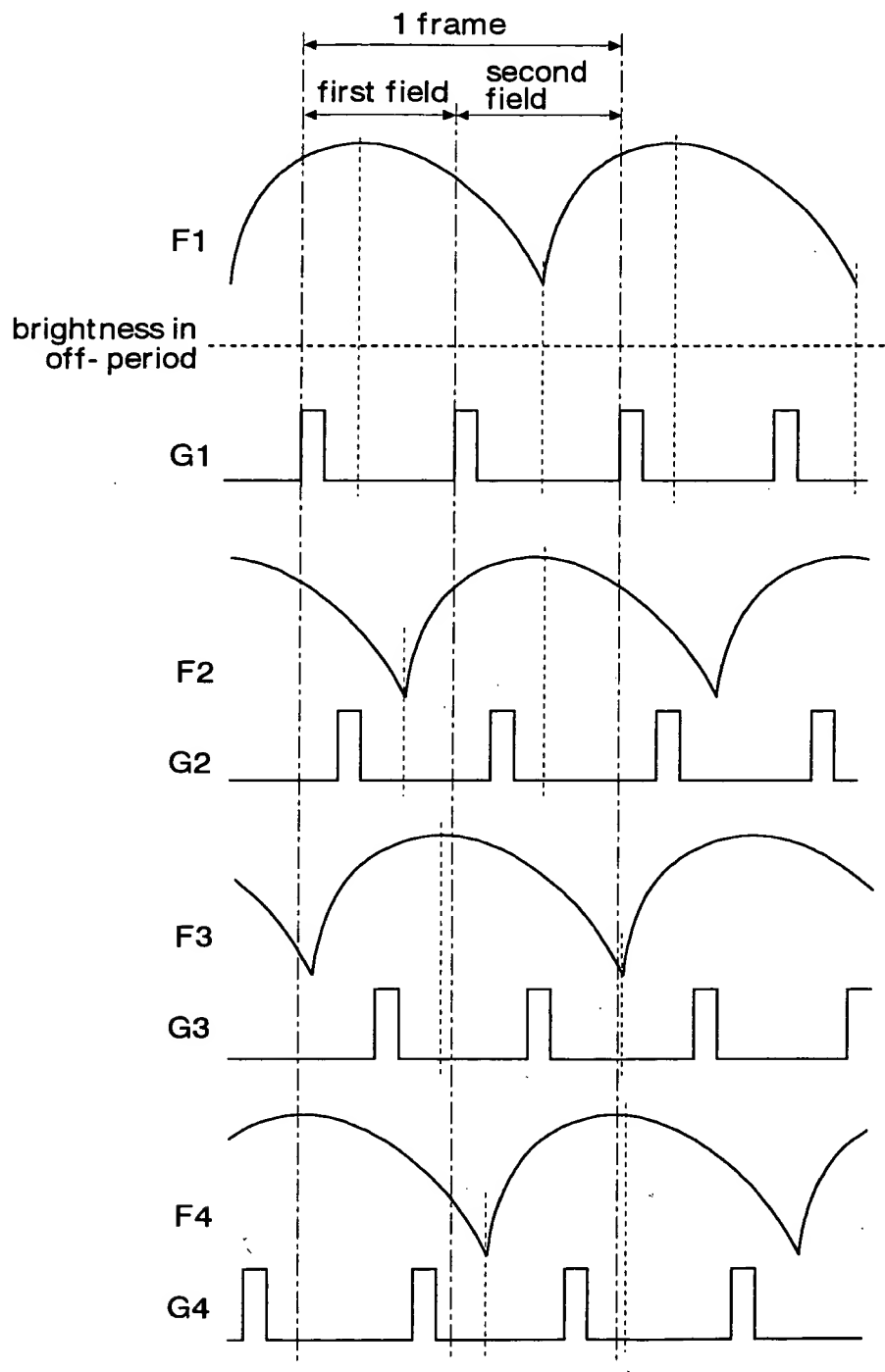


Fig. 20

Fig. 21

Fig. 22

Timing diagram for gate signals G1 through G8. The diagram shows a 16ms frame divided into two 8ms fields. Gate signals G1 through G8 are shown as pulses. G1 and G8 are active during the first field, while G2 through G7 are active during the second field. The diagram is labeled "gate signal (scanning line)" on the left.

Fig. 23

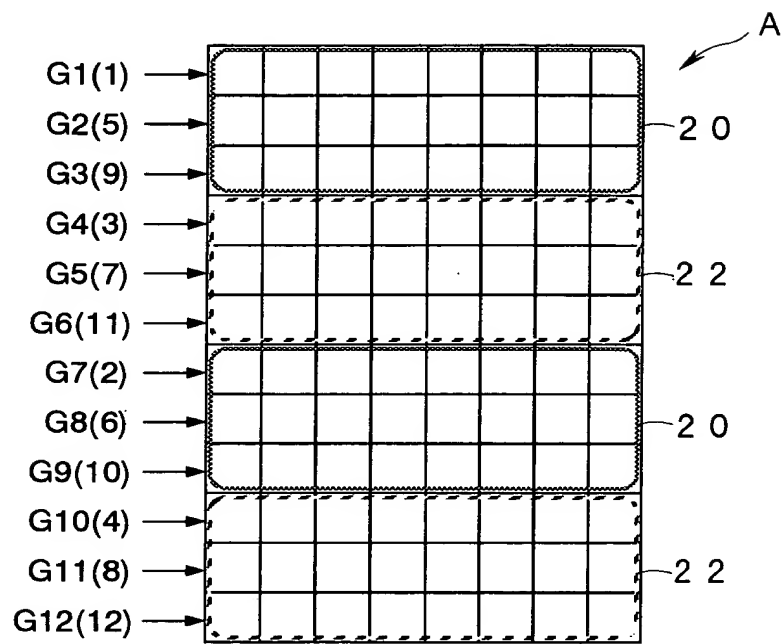


Fig. 24

09661483-03000

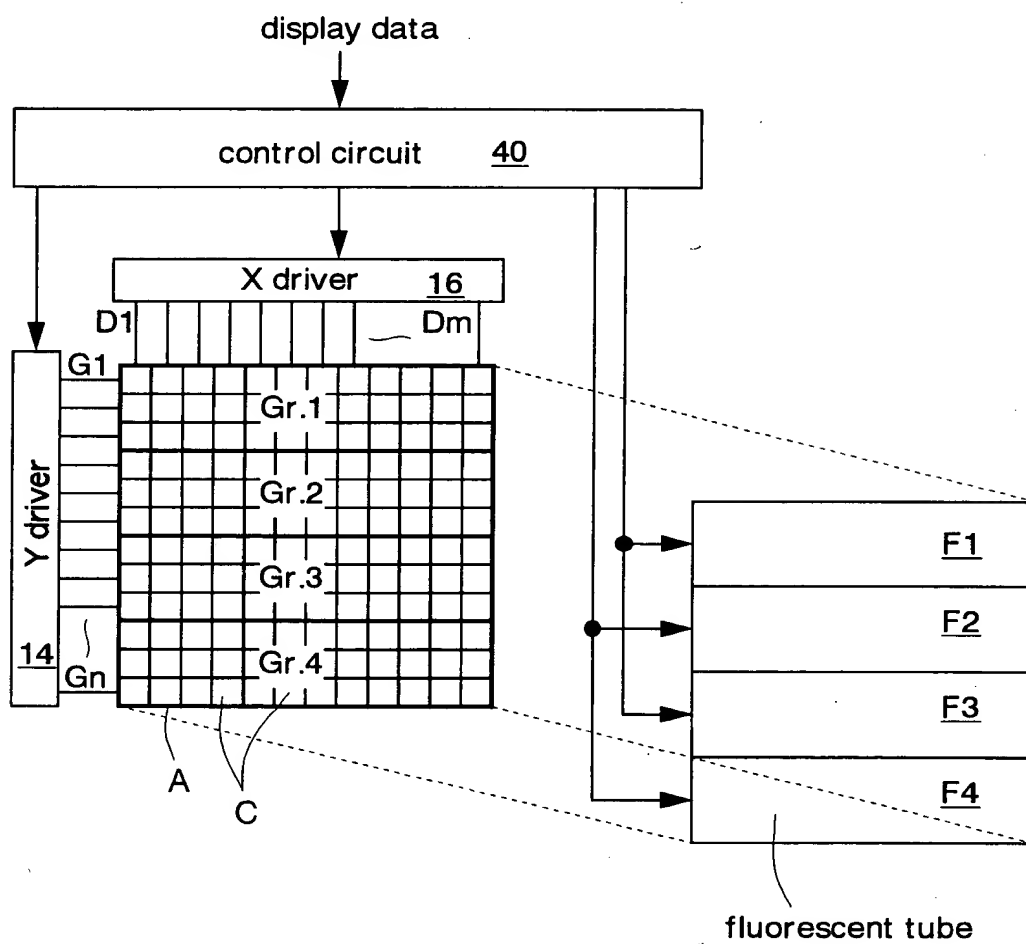


Fig. 26

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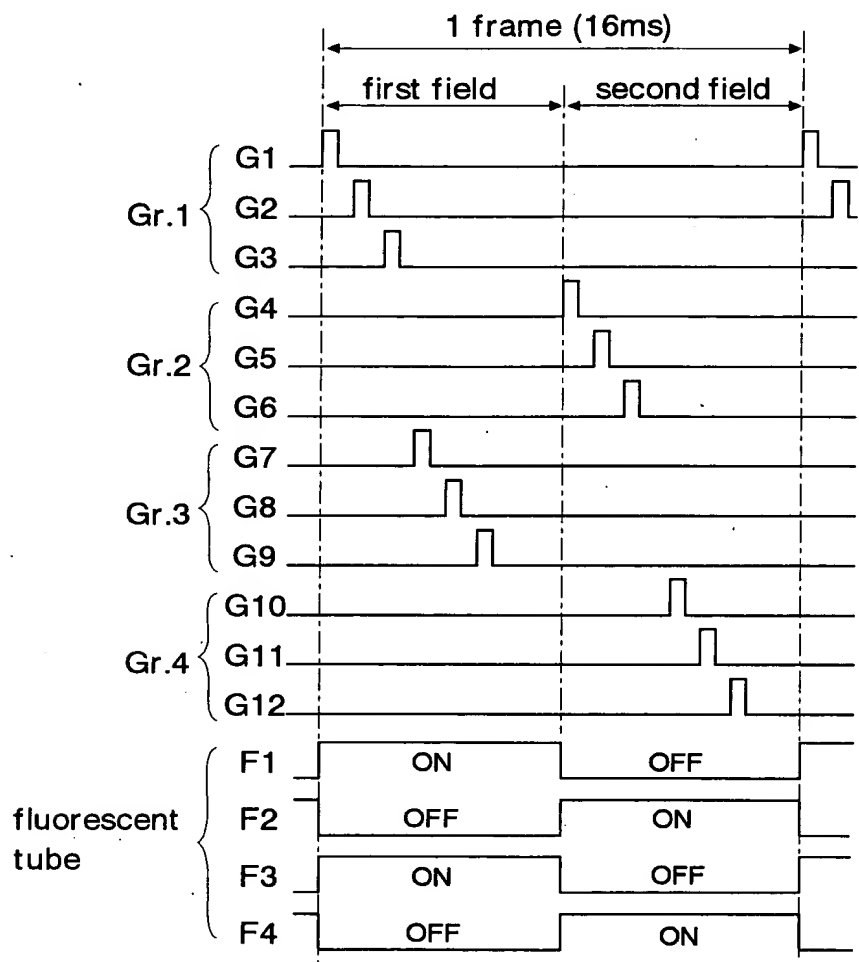


Fig. 27

fluorescent tube

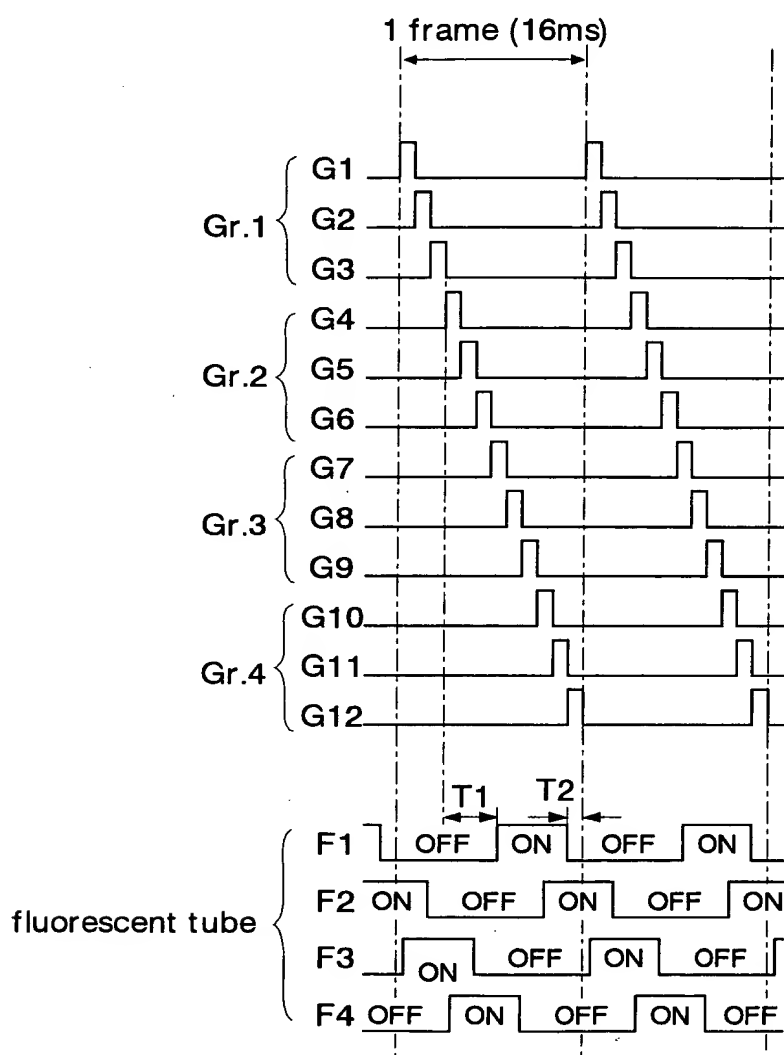


Fig. 29

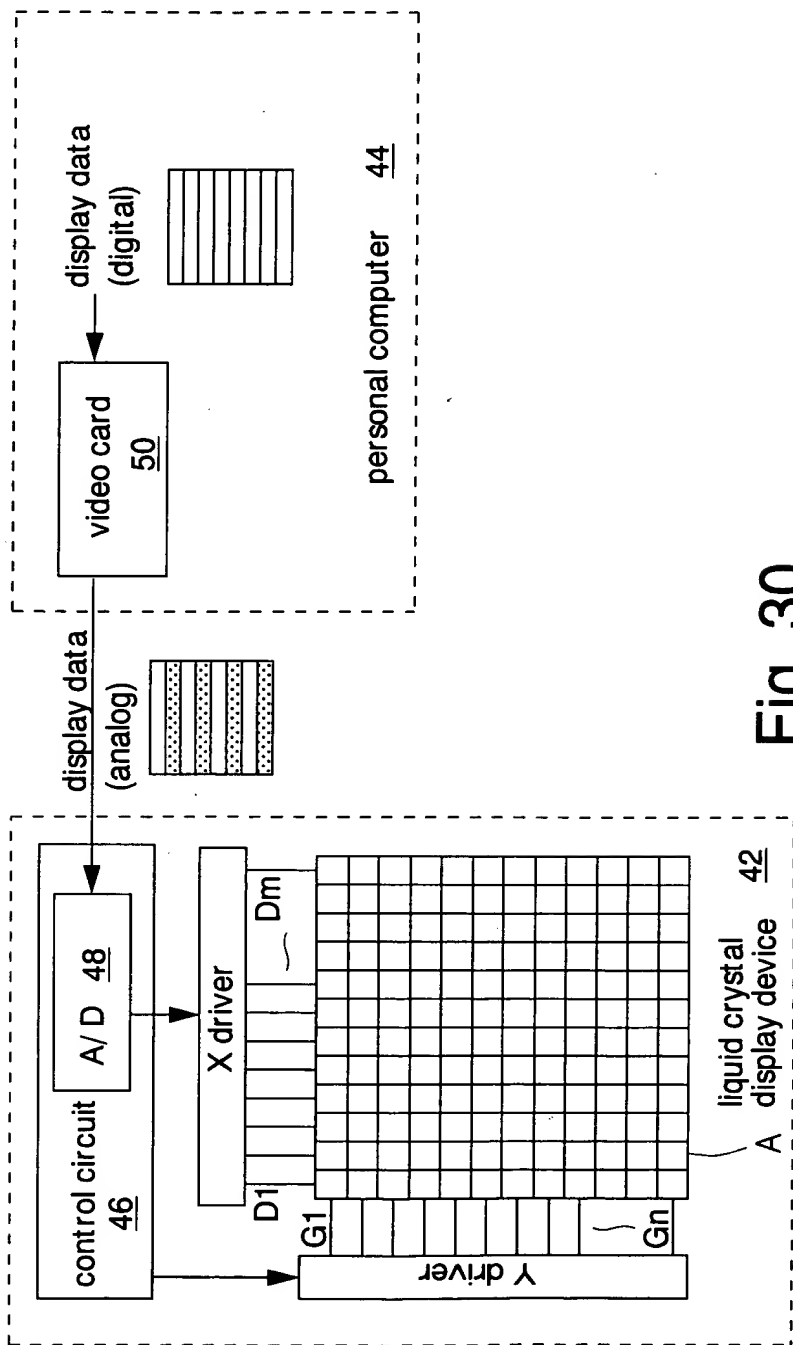


Fig. 30

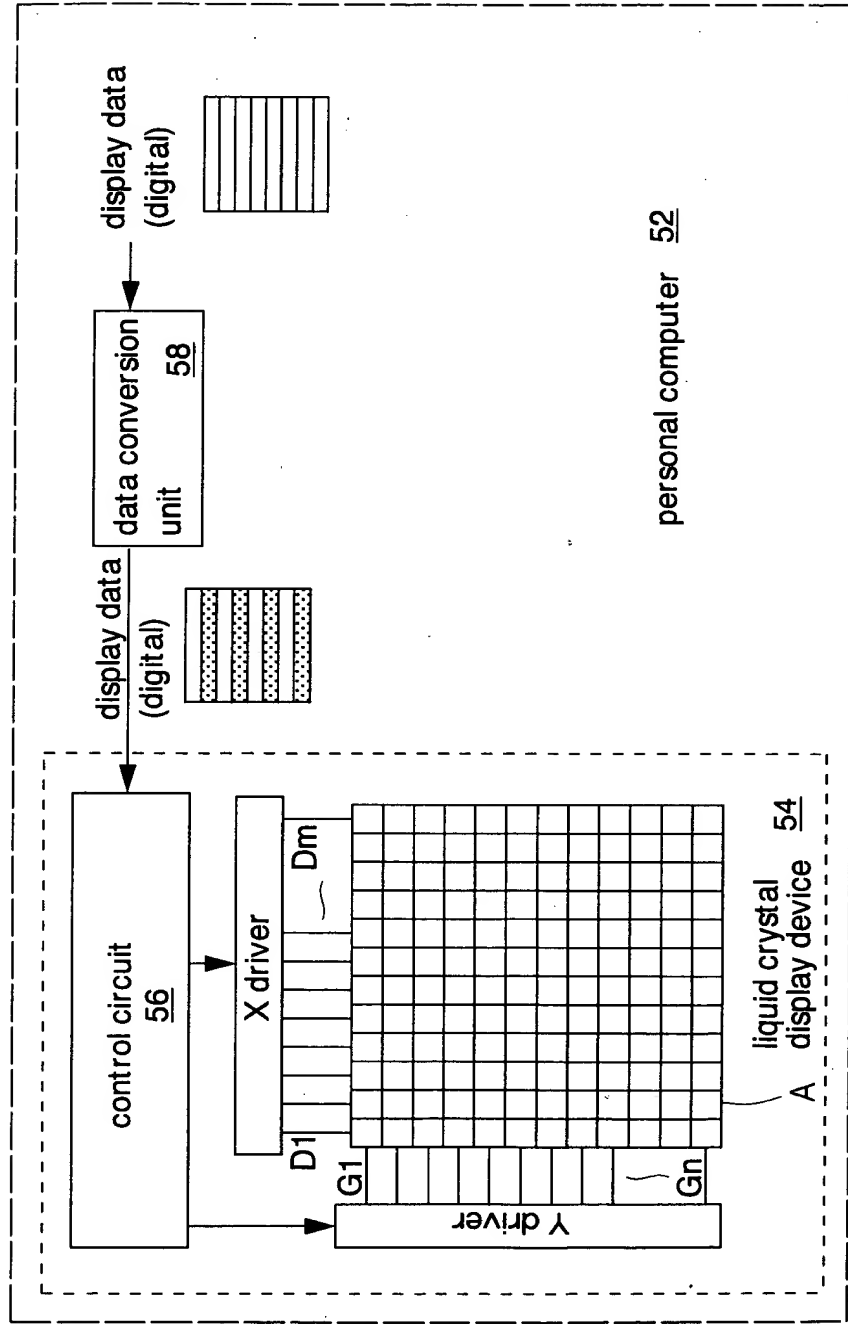


Fig. 31

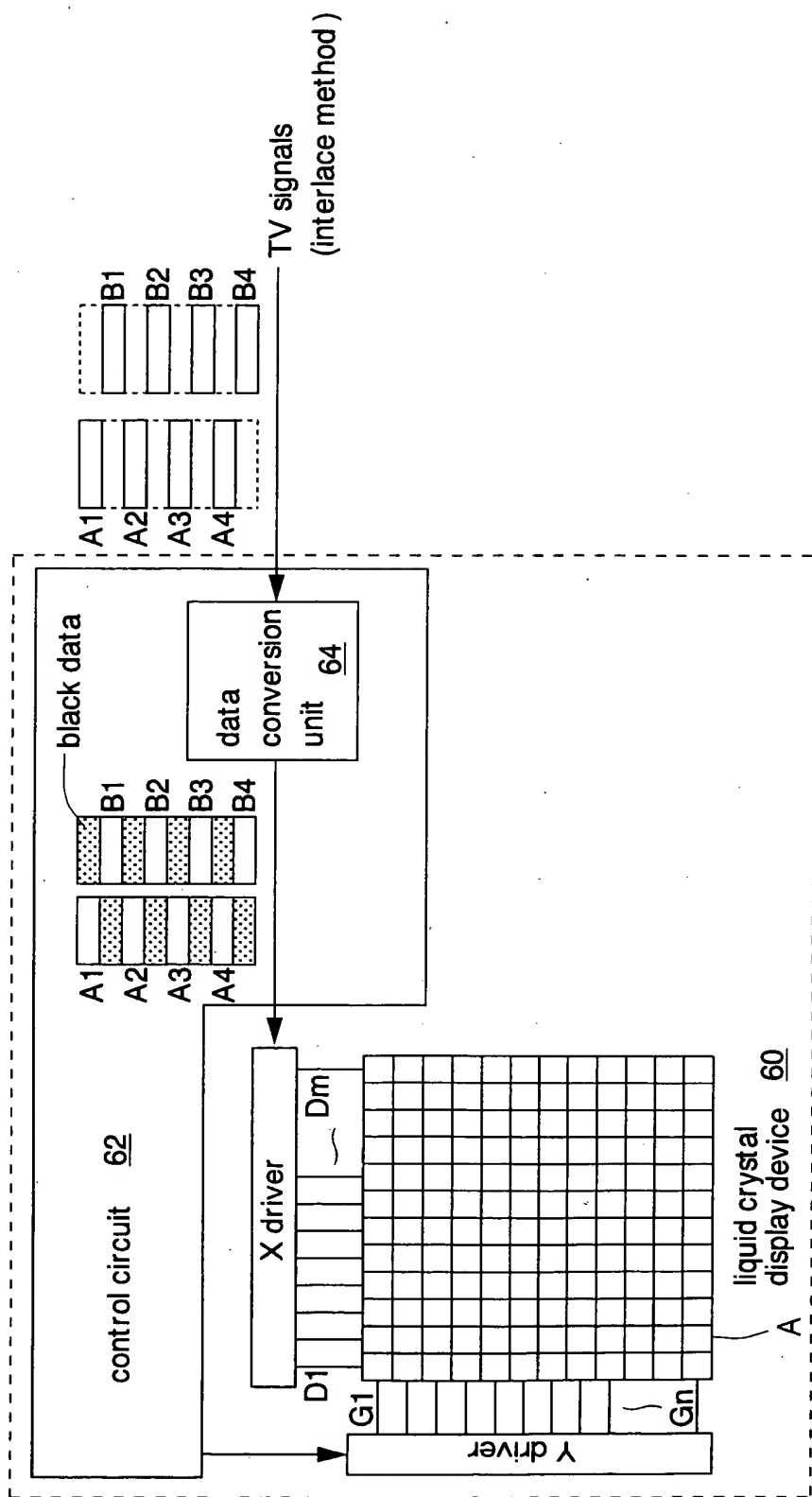


Fig. 32

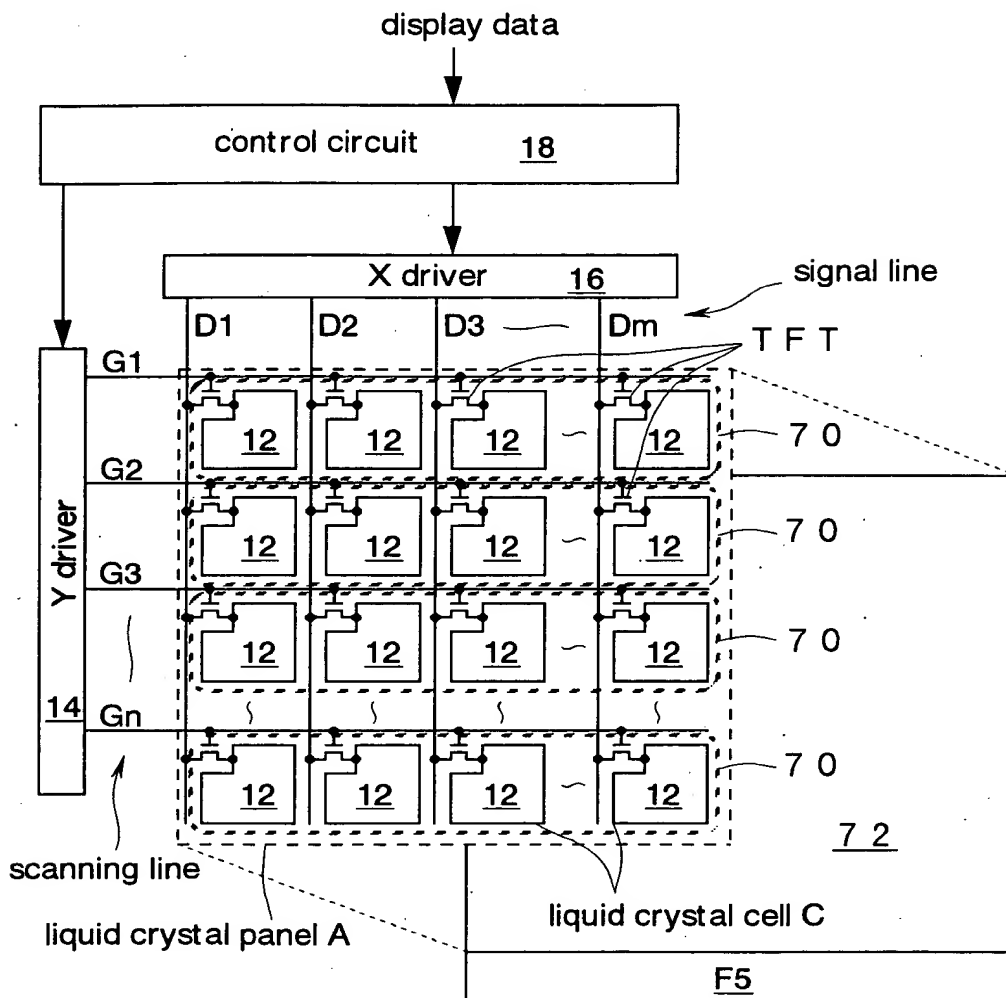


Fig. 33

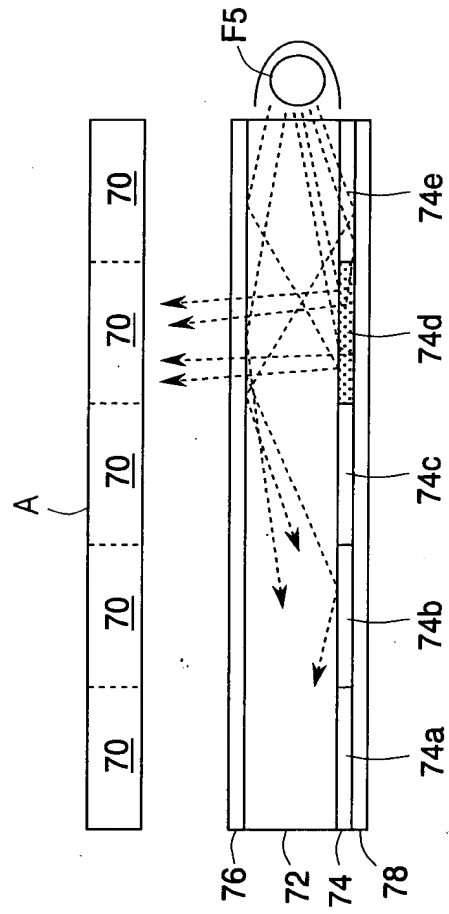


Fig. 34

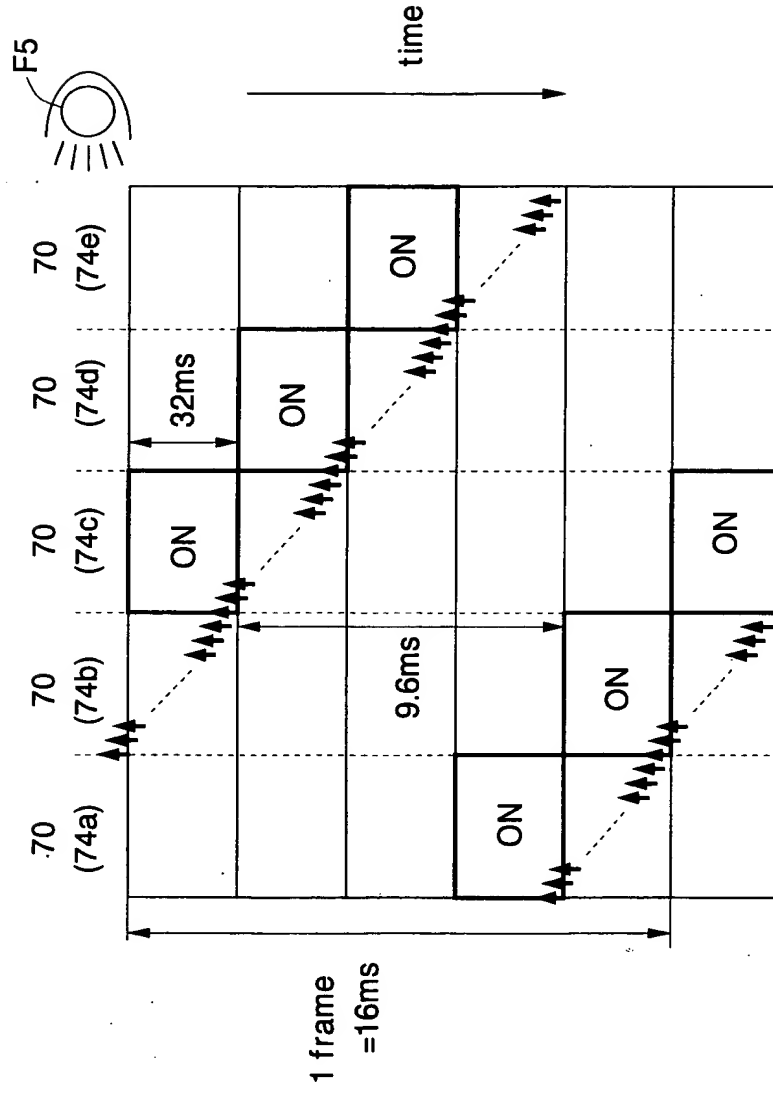


Fig. 35

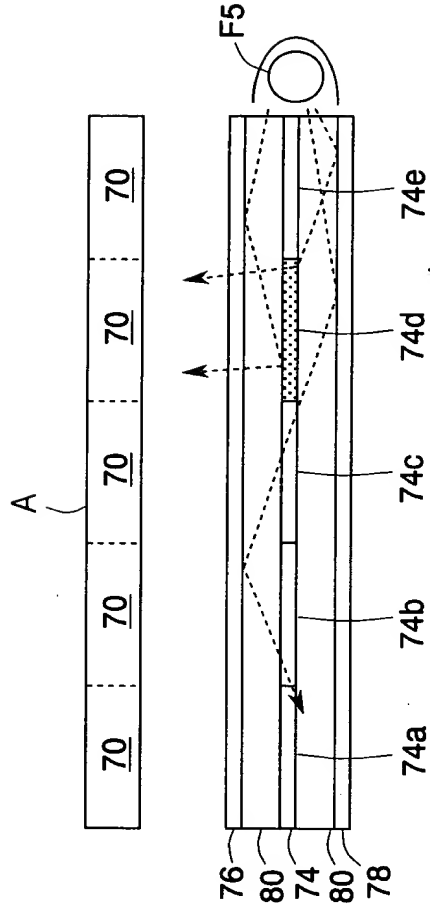


Fig. 36

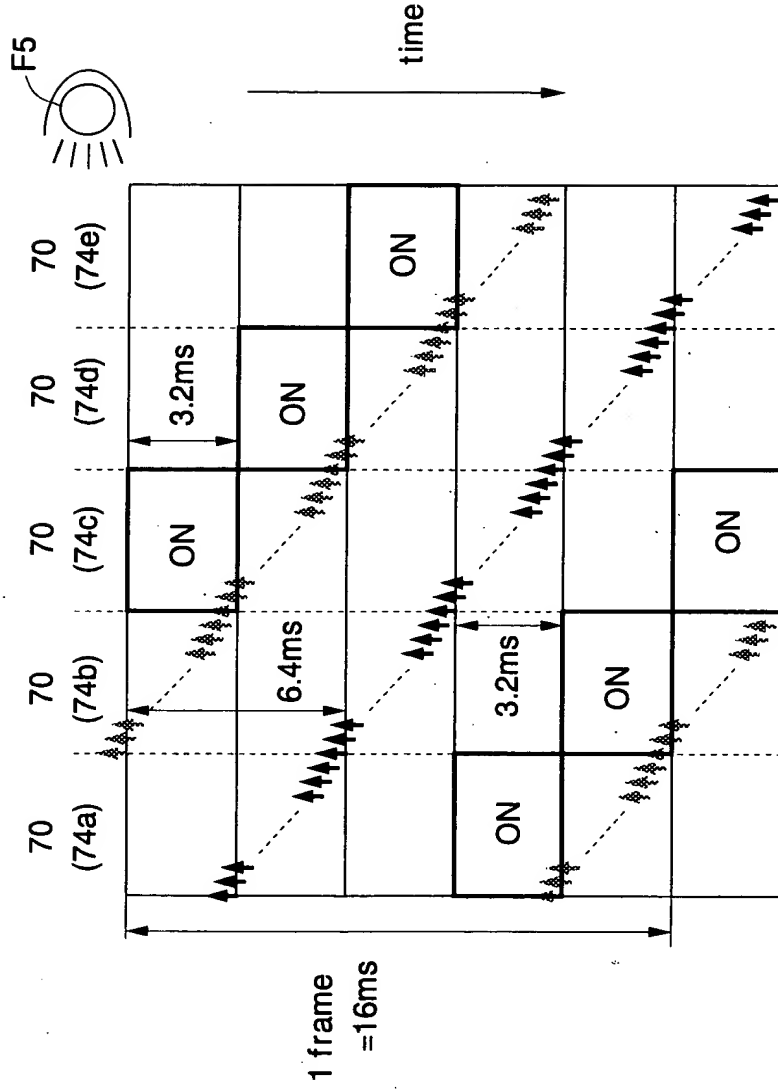


Fig. 37

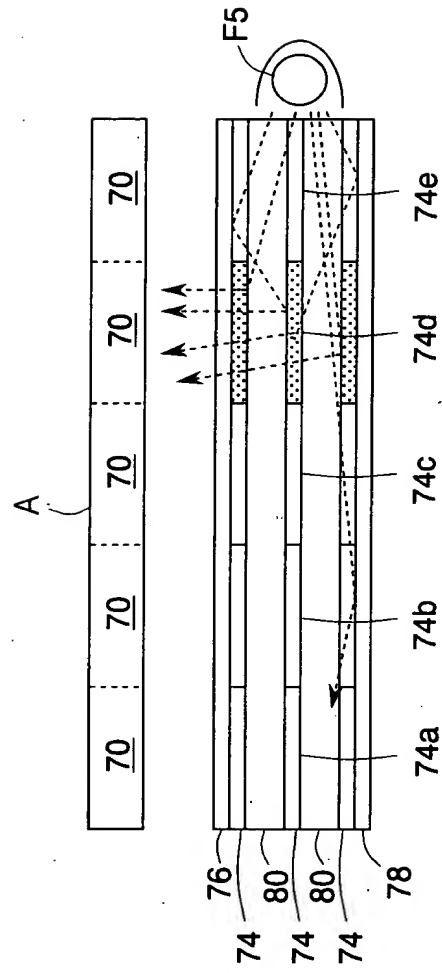


Fig. 38

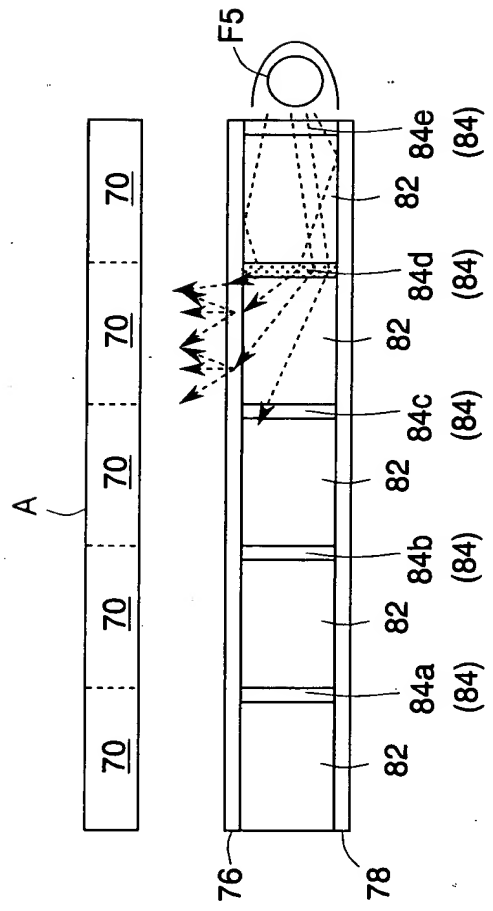


Fig. 39

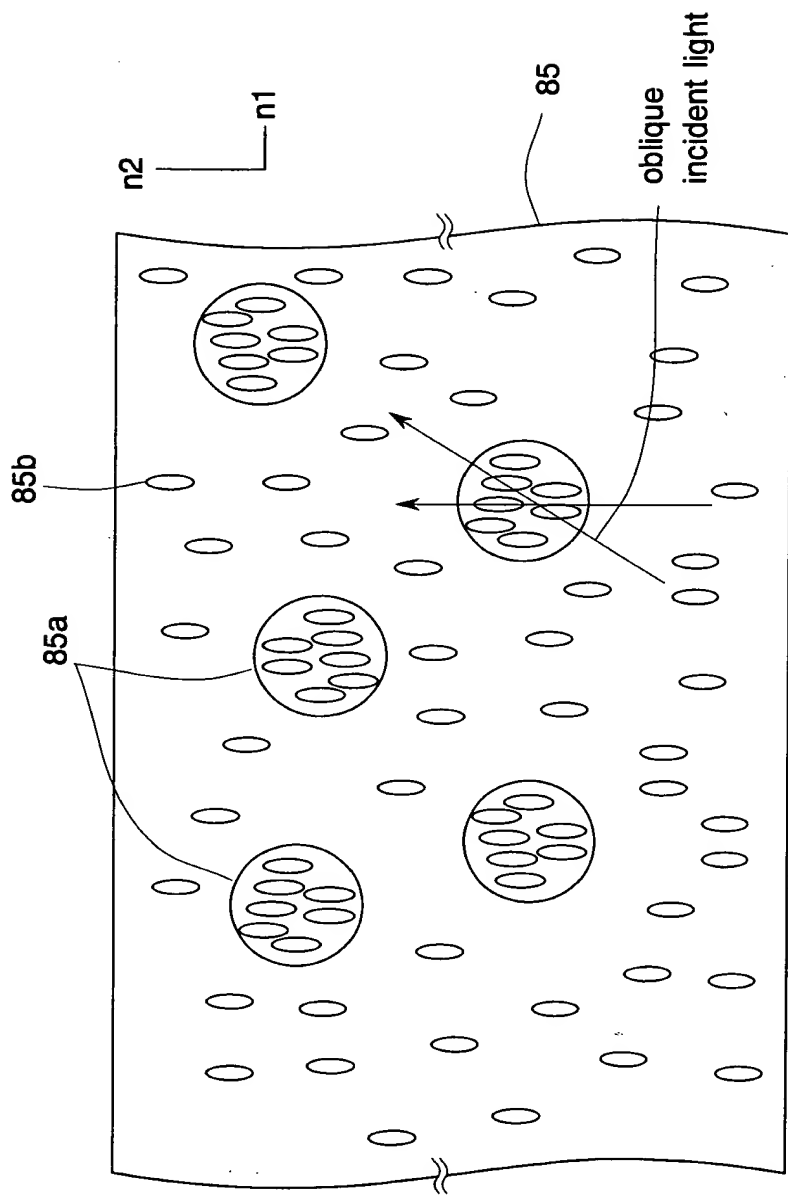


Fig. 40

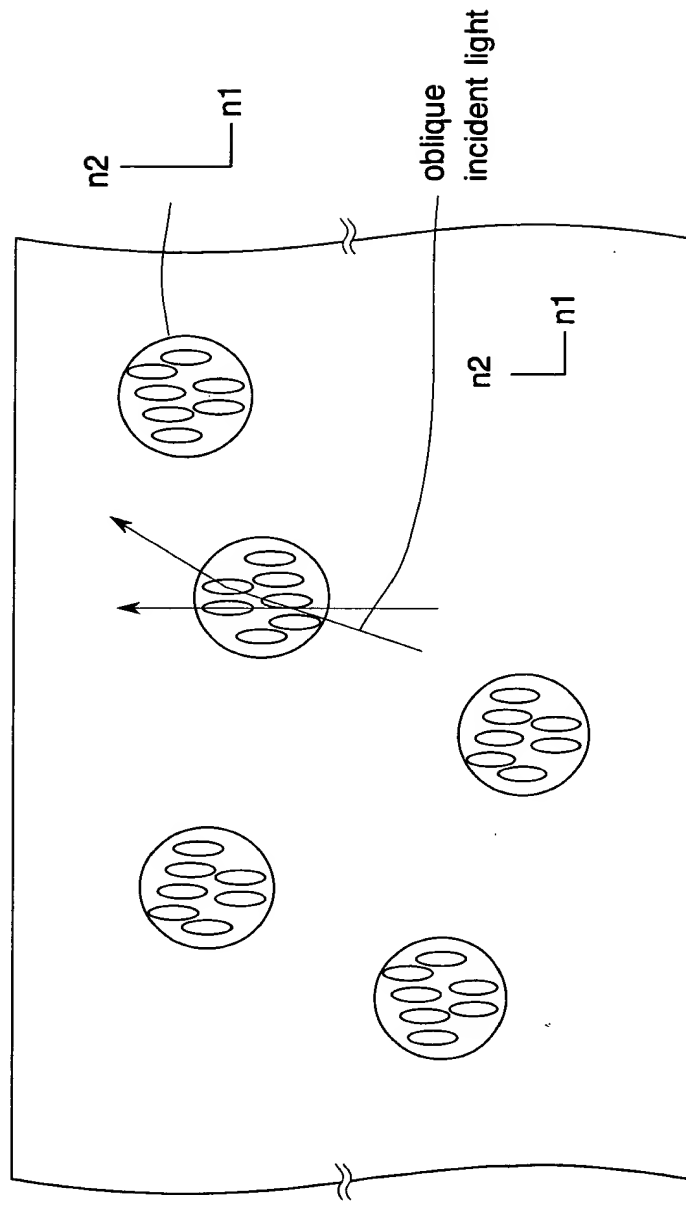


Fig. 41

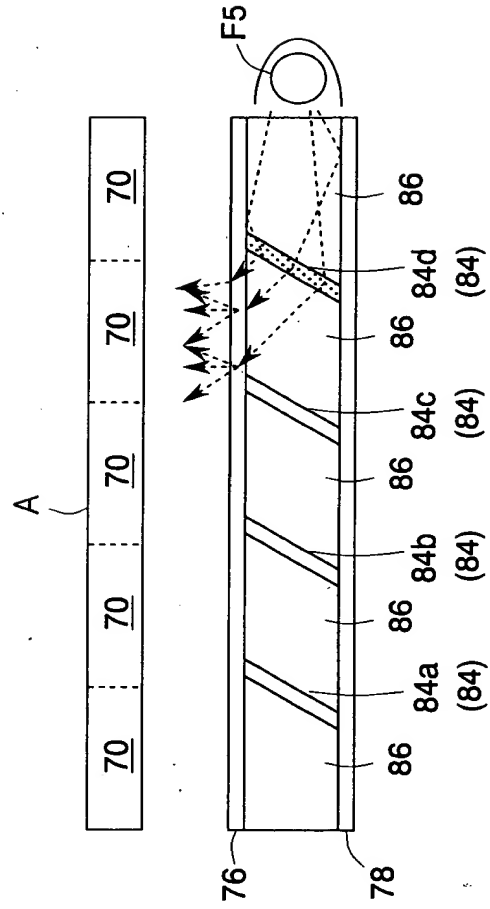


Fig. 42

display data

control circuit 90

SW

X driver 16

D1 Dm

Y driver 14

G1 Gn

A C

luminescent period

data black

1 frame period

74a

74b

72 74c

74d

74e

F5

80

Fig. 43

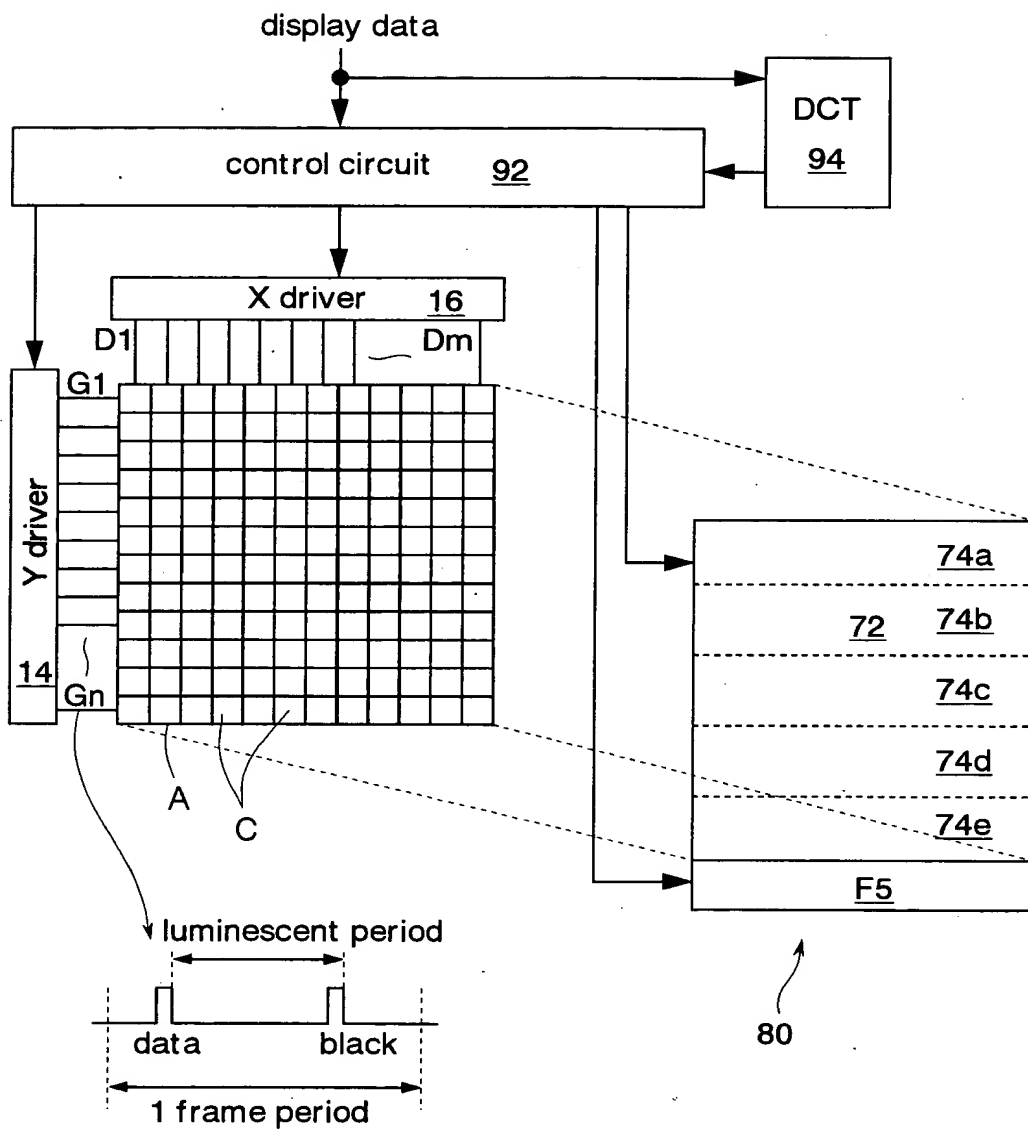


Fig. 44

display data

control circuit 96

X driver 16

D1 Dm

Y driver

G1 Gn

14

A C

74a

72 74b

74c

74d

74e

F5

80

Fig. 45

80

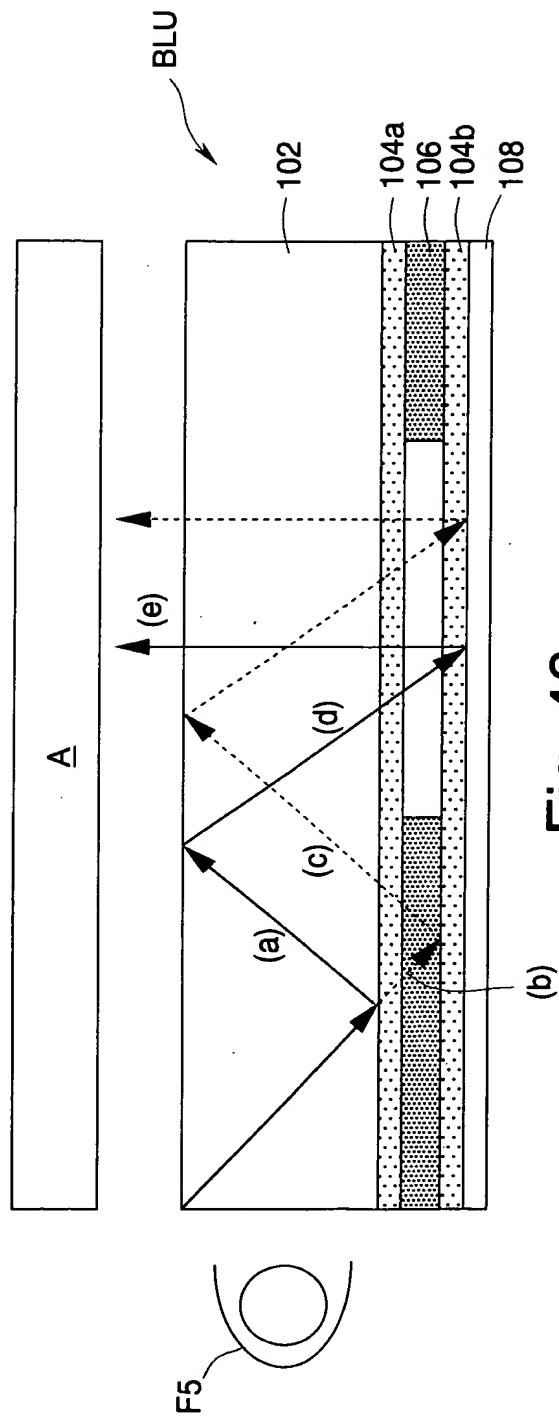


Fig. 46

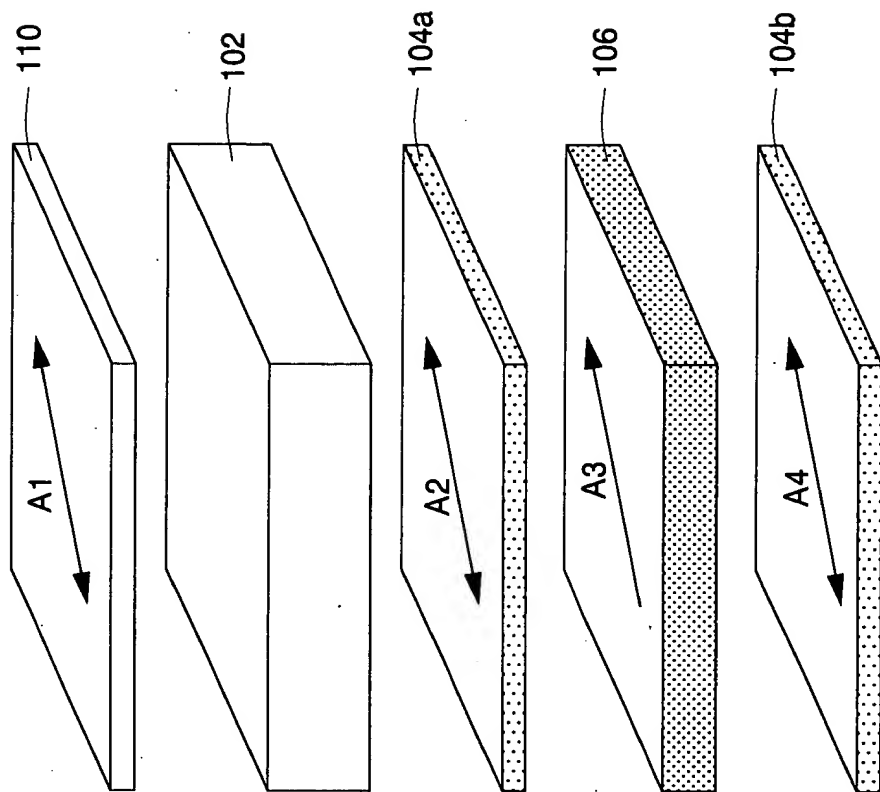


Fig. 48

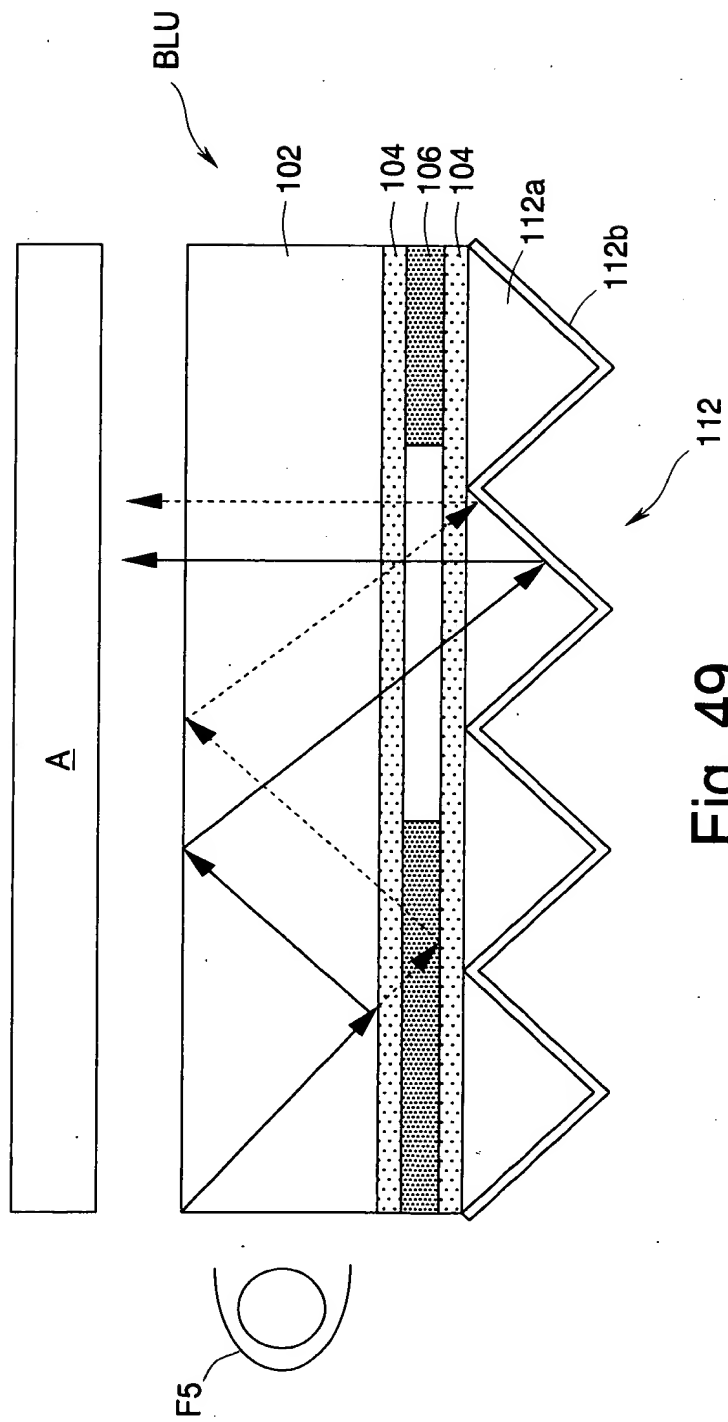


Fig. 49

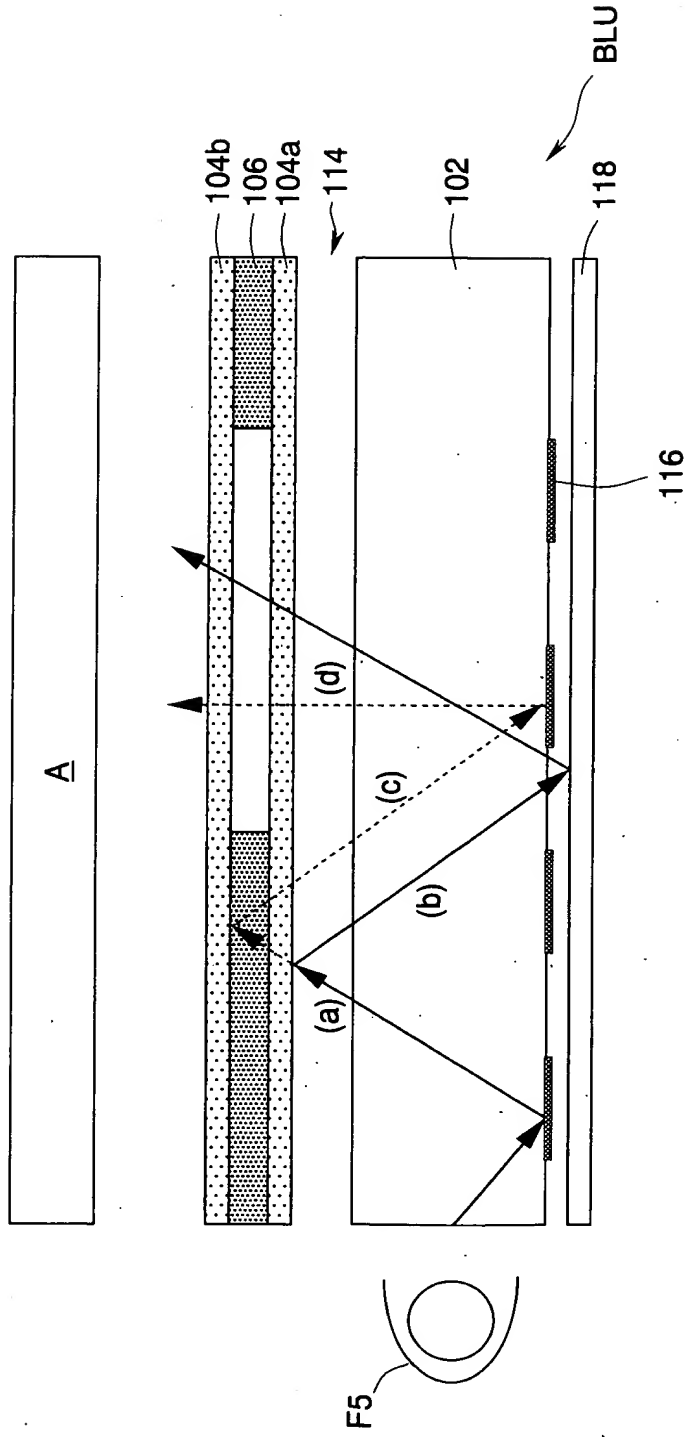


Fig. 52

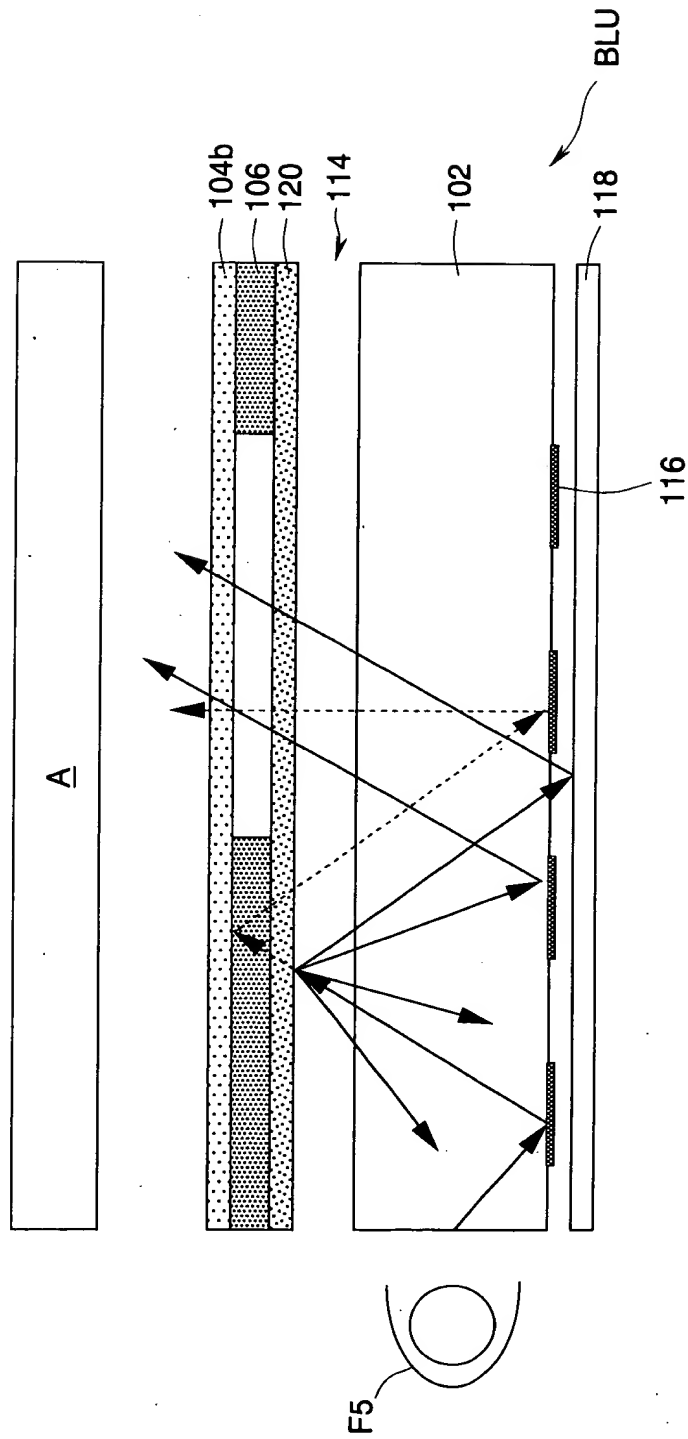


Fig. 53

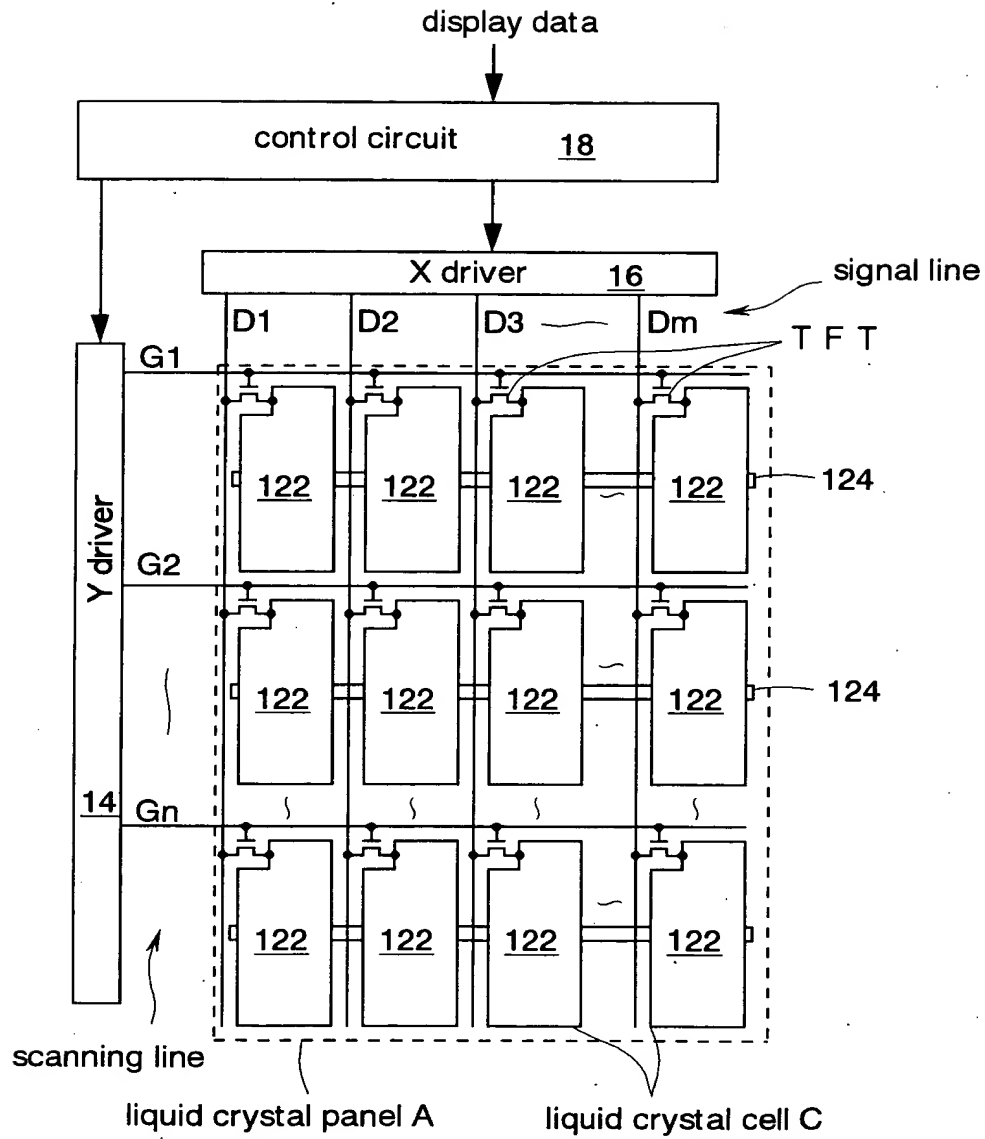


Fig. 54

Fig. 55

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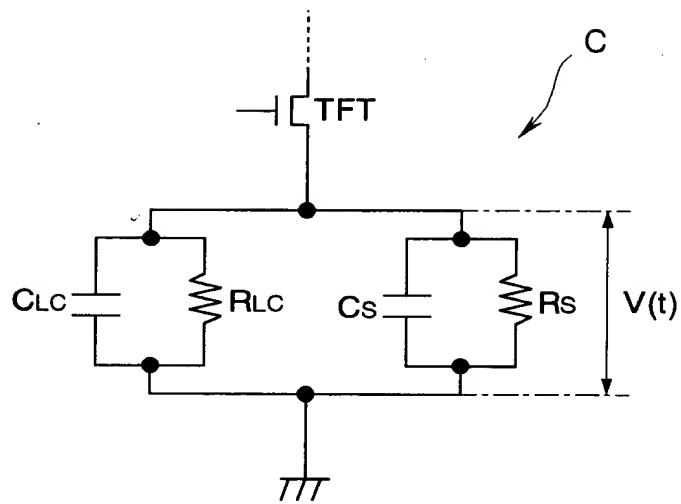


Fig. 56

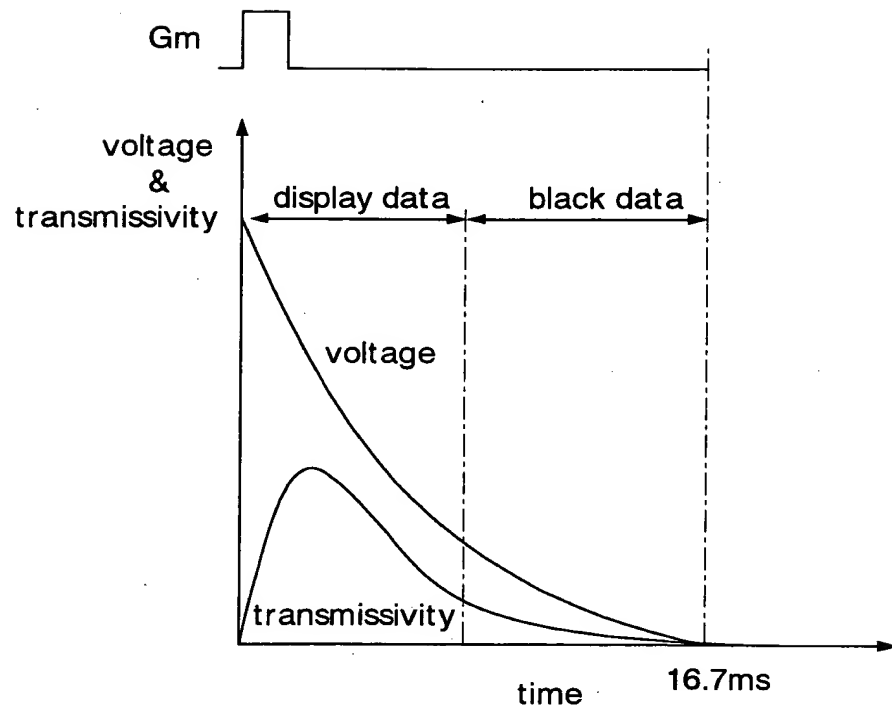


Fig. 57

The graph shows the voltage $V(t)$ in percent on the y-axis (0 to 100) against time in milliseconds on the x-axis (0 to 20). Six exponential decay curves are plotted, each corresponding to a different time constant: 1.0, 0.1, 0.05, 0.01, 0.005, and 0.001 ms. A vertical dashed line at 16.7 ms is indicated by an arrow and labeled '16.7ms'.

Time [ms]	1.0 ms	0.1 ms	0.05 ms	0.01 ms	0.005 ms	0.001 ms
0	100	100	100	100	100	100
5	98	92	85	60	20	2
10	96	84	70	35	10	0
15	94	76	60	22	5	0
16.7	93	72	55	20	4	0
20	92	68	50	18	3	0

Fig. 58

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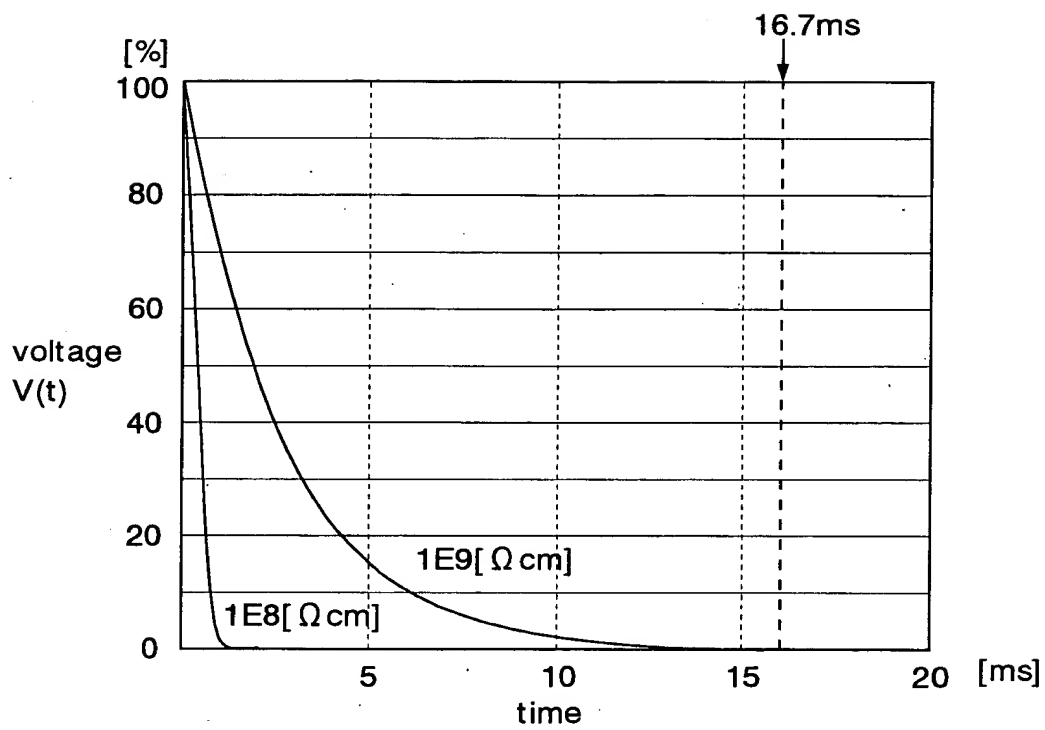


Fig. 59

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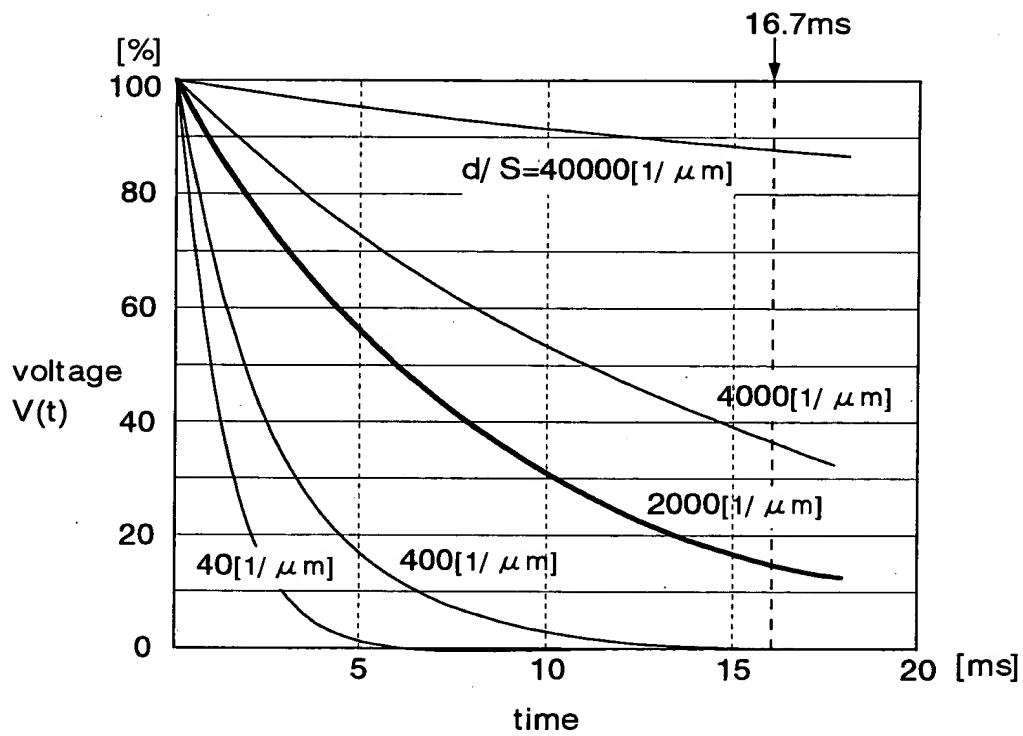


Fig. 60

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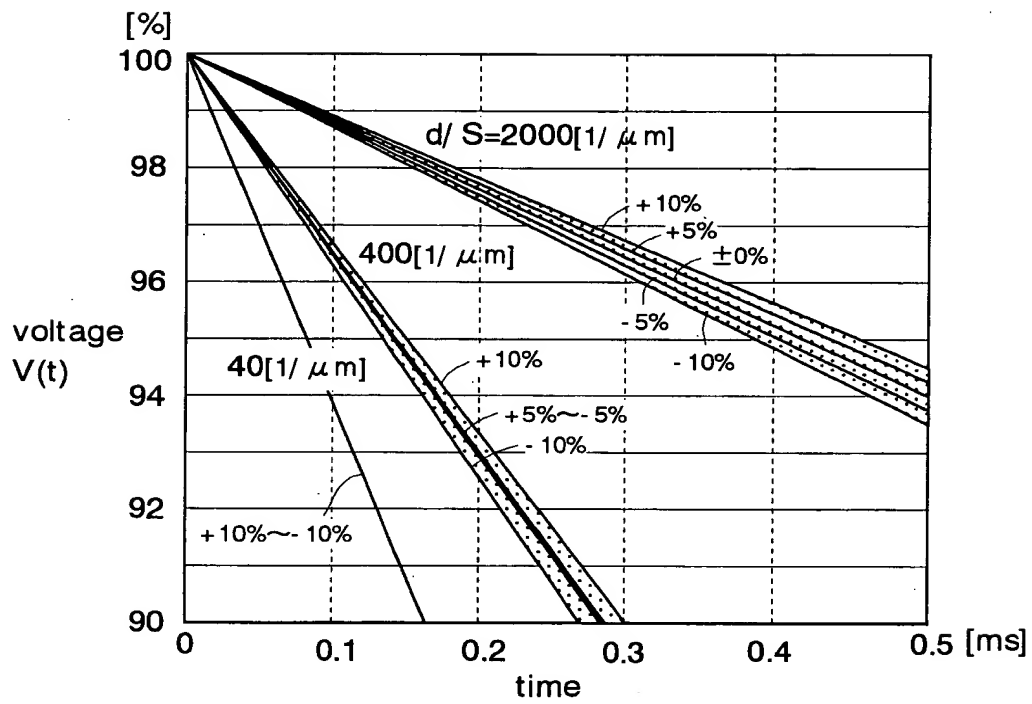


Fig. 61

Fig. 62

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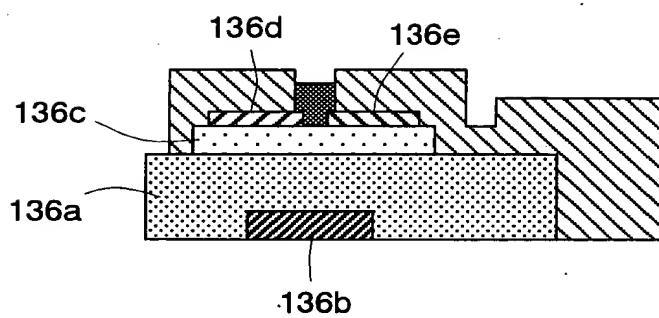


Fig. 63

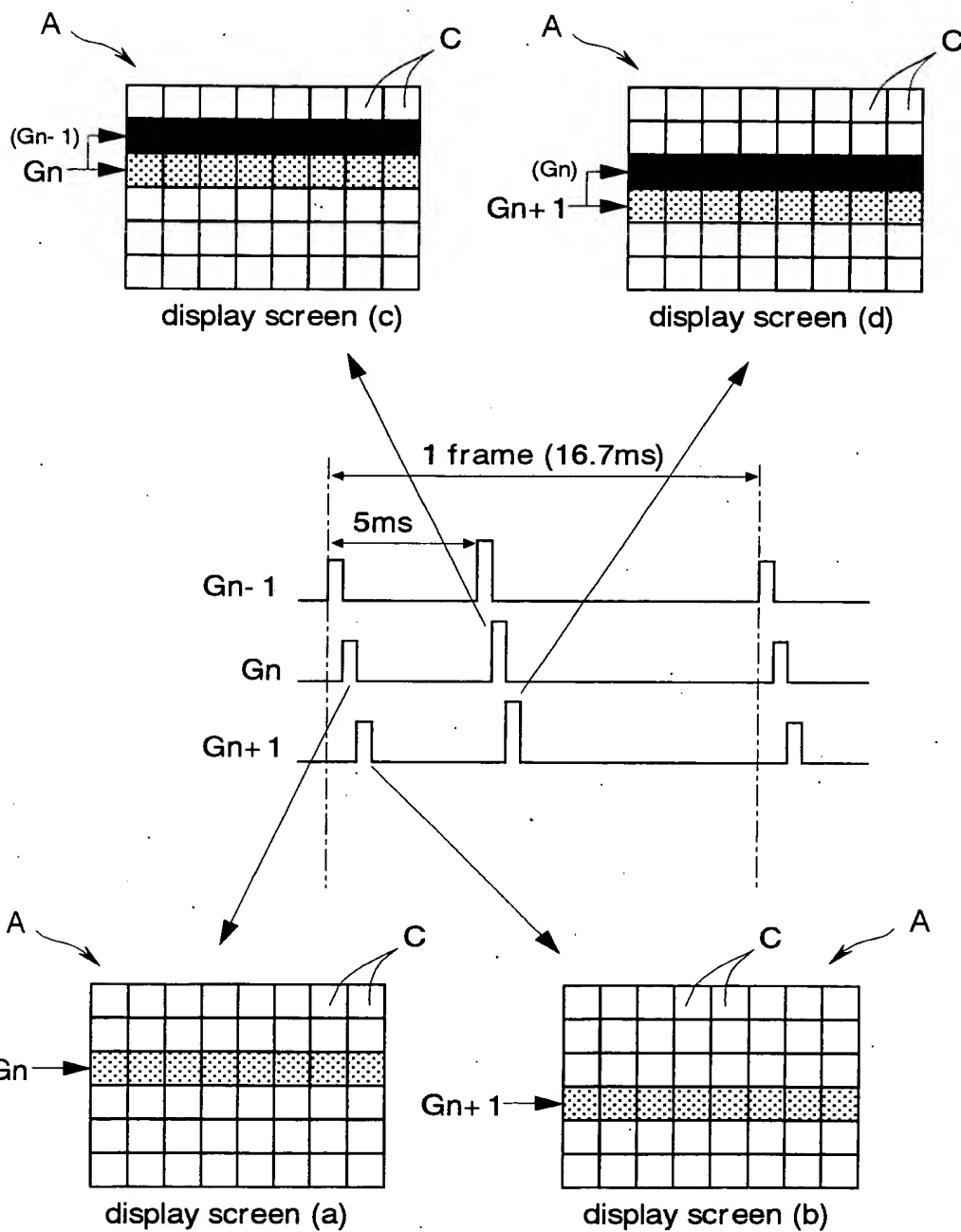


Fig. 64

Fig. 65

DT BL

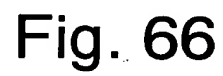


Fig. 66

Fig. 67

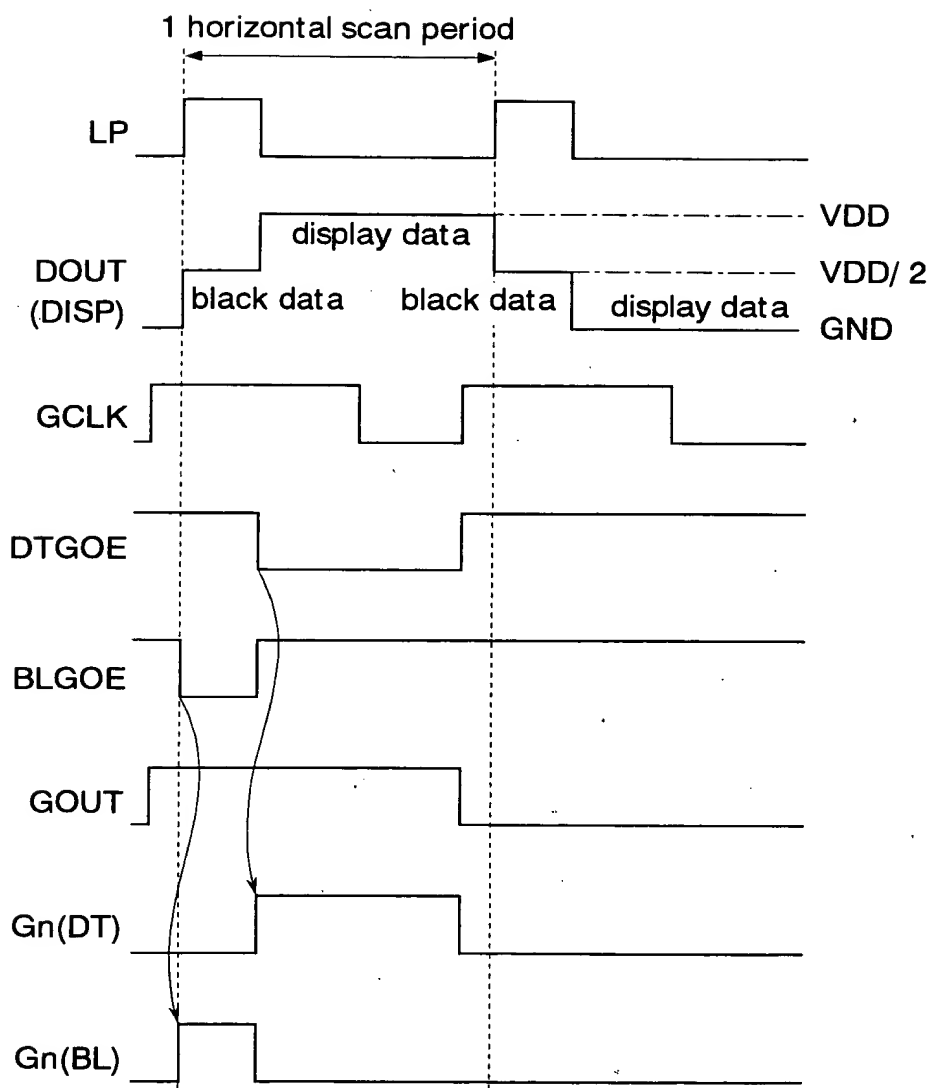


Fig. 68

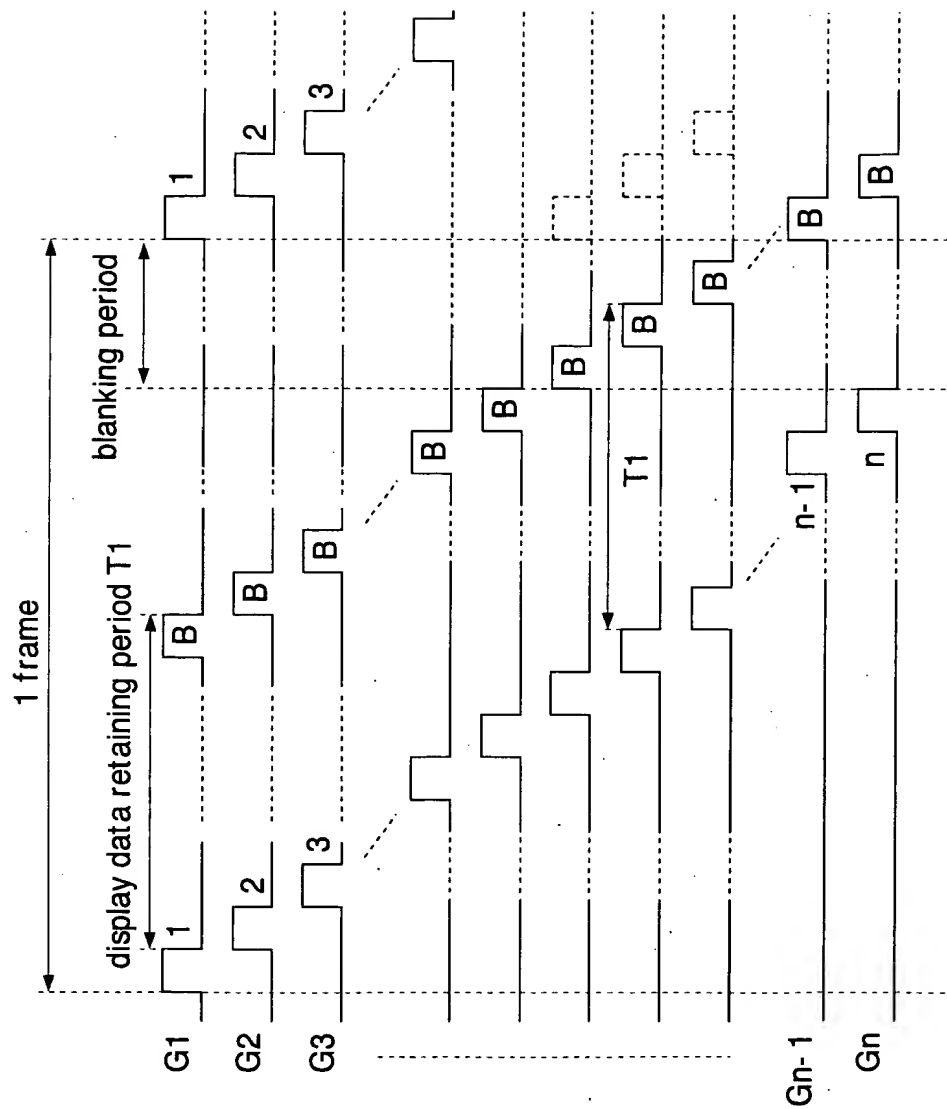


Fig. 69

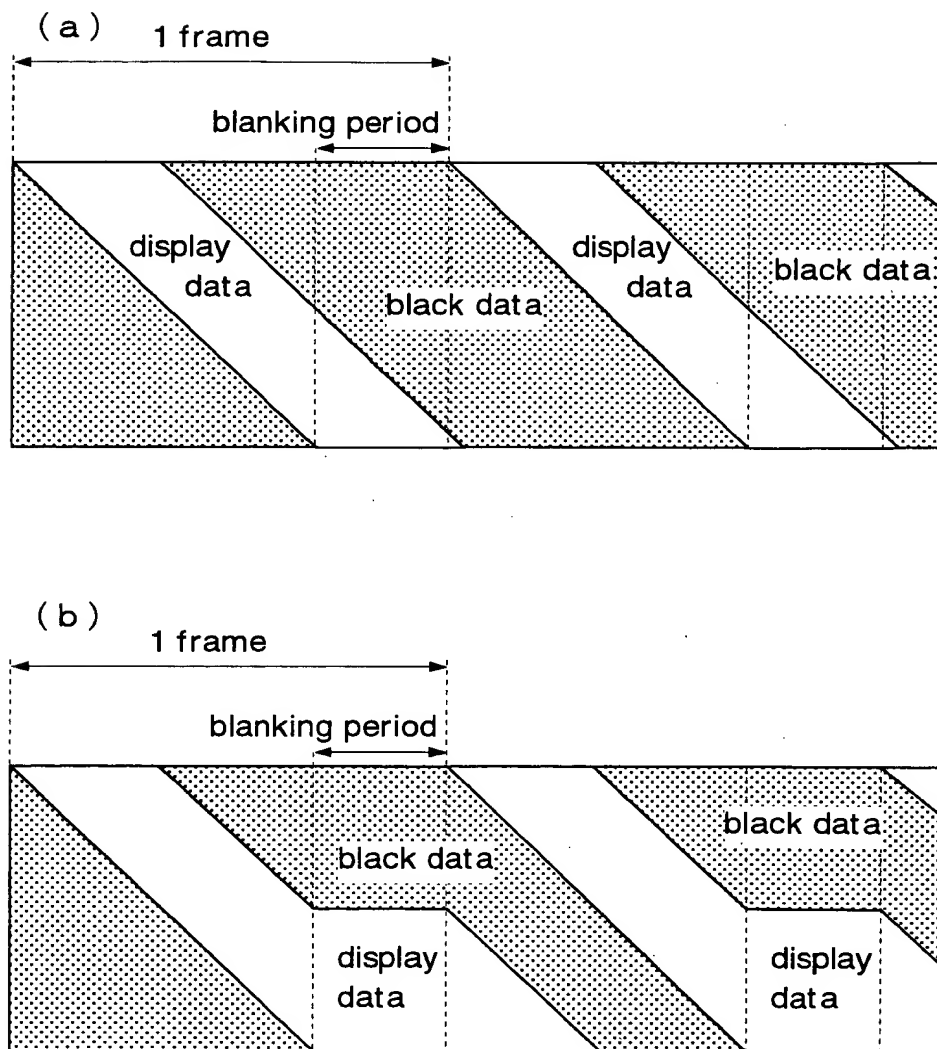


Fig. 70

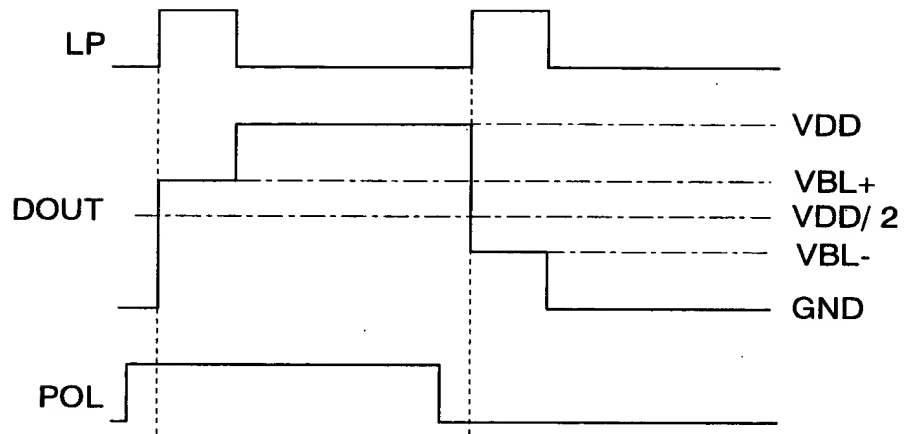


Fig. 71

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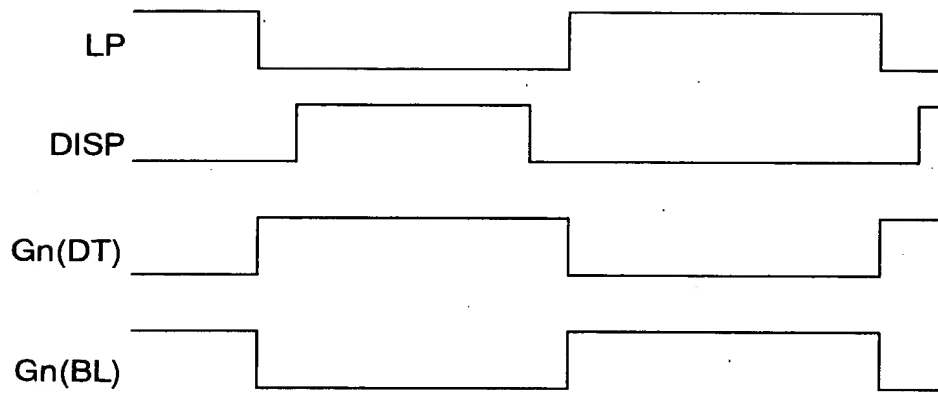


Fig. 72

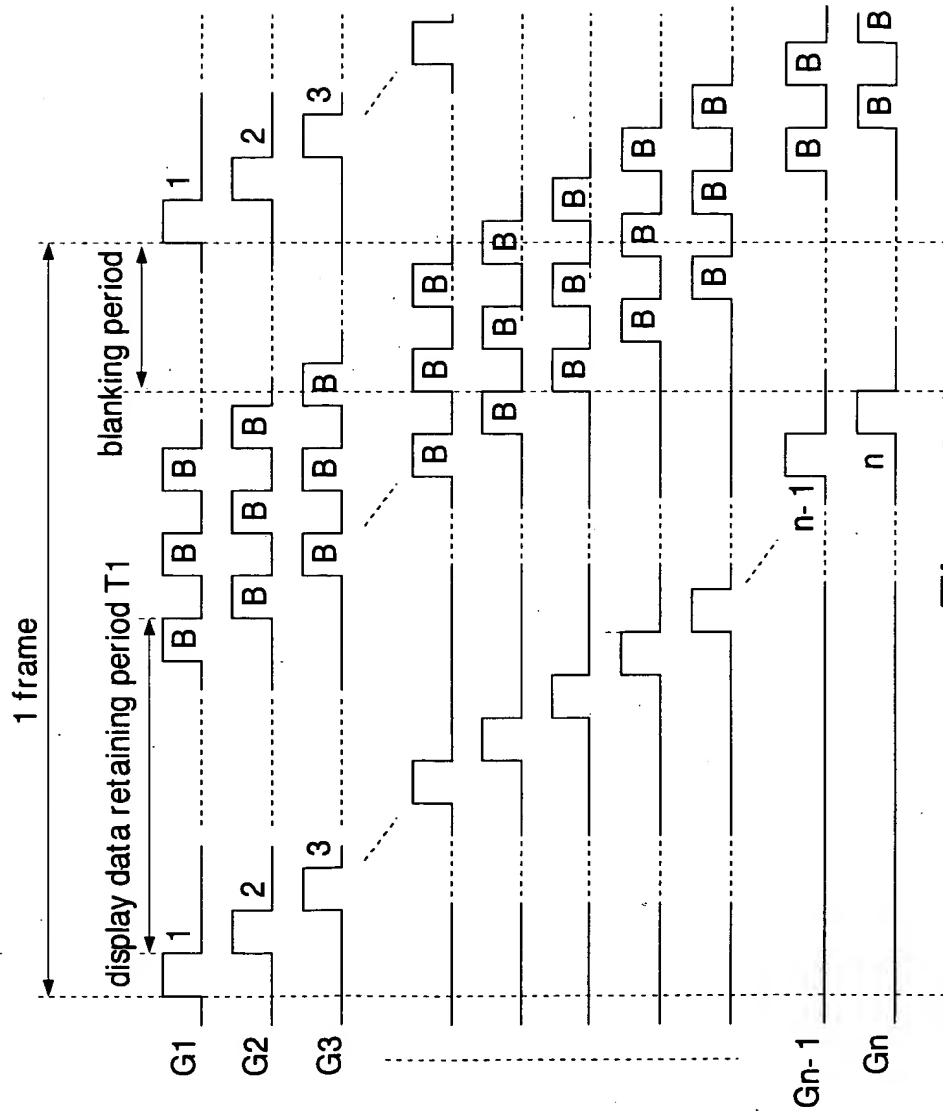


Fig. 73

Fig. 74

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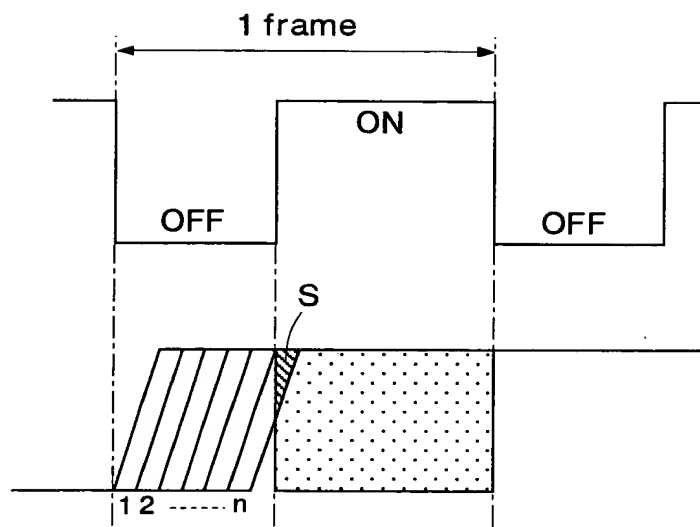


Fig. 75

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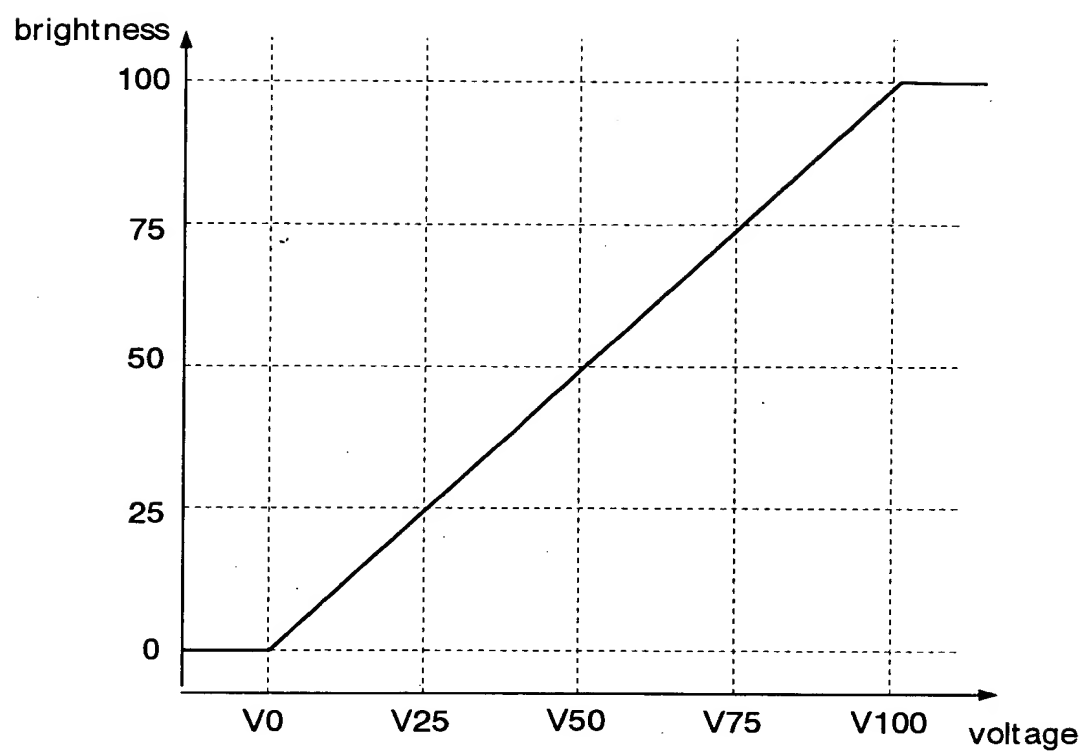


Fig. 76

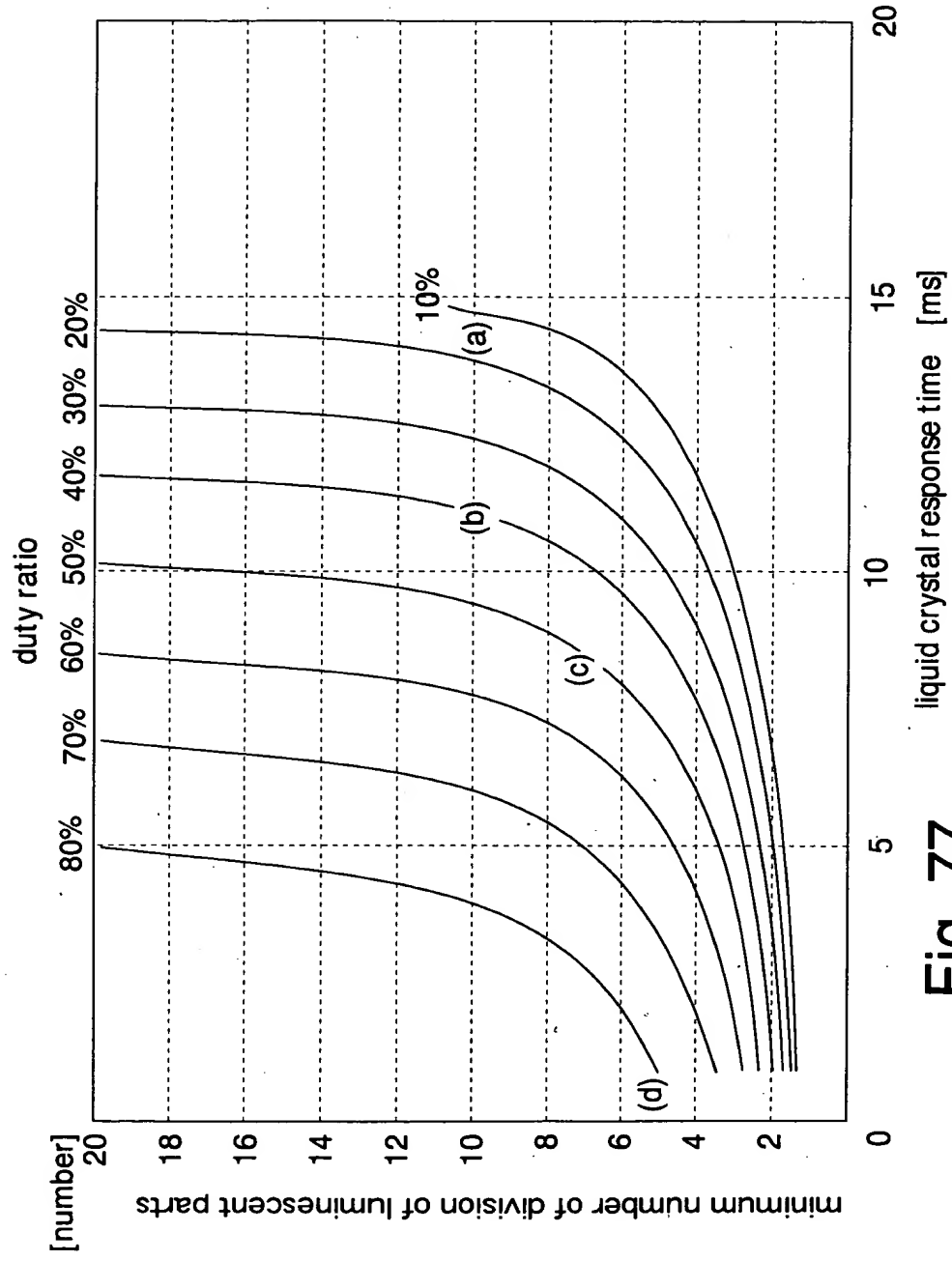


Fig. 77

The diagram illustrates the architecture of a display system. At the top, "display data" is input into a "control circuit 142". The control circuit 142 is connected to an "X driver 16" and a "Y driver 14". The X driver 16 is connected to a grid of pixels, with horizontal lines labeled D1, Dm, and Gn. The Y driver 14 is connected to the same grid, with vertical lines labeled G1 and Gn. The grid is composed of a series of horizontal lines A and vertical lines C. A detailed view of the grid is shown in the bottom right, labeled 144a, which shows a series of horizontal lines (1) through (9) and a vertical line 146. The entire system is labeled 144.

Fig. 78

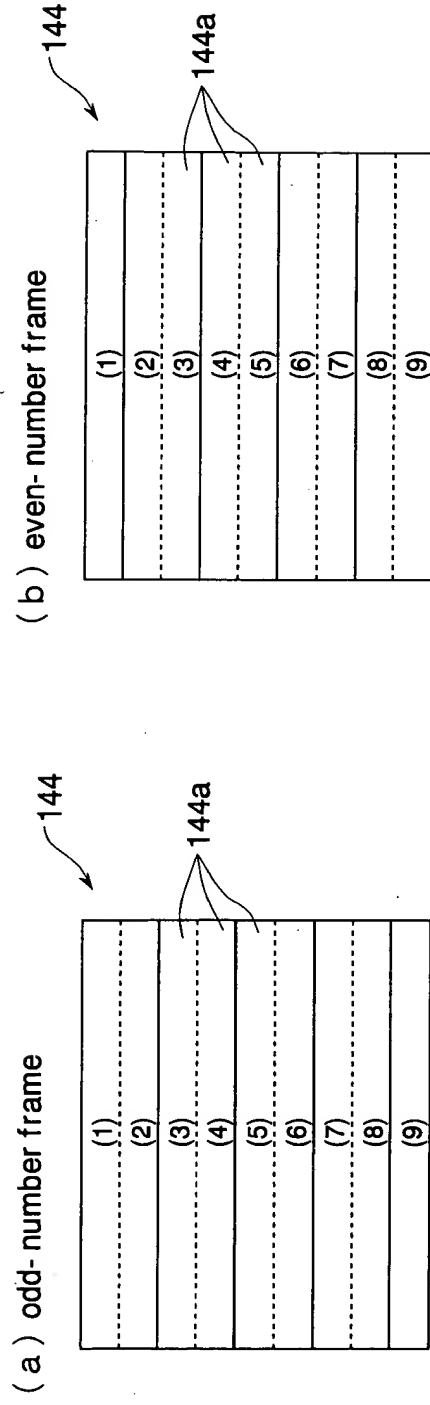


Fig. 79

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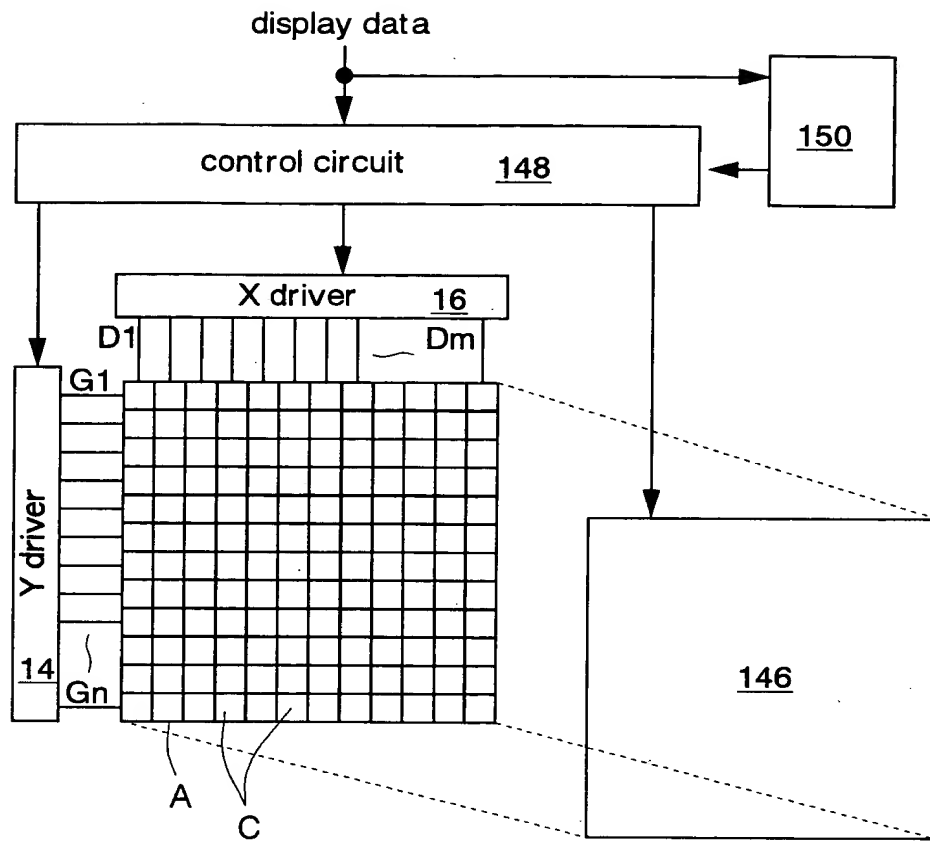


Fig. 80

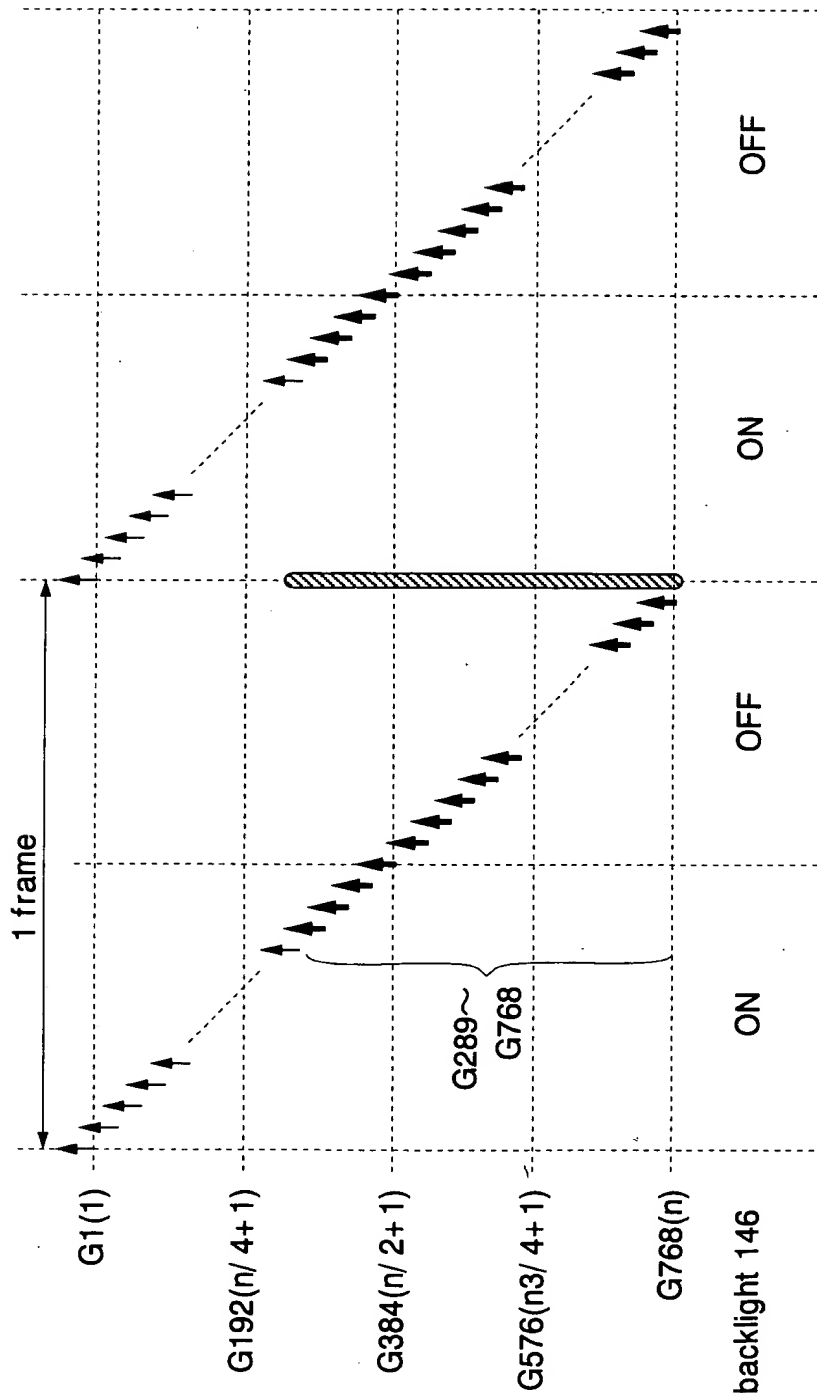


Fig. 81

Fig. 82